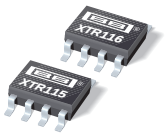
Burr-Brown Products from Texas Instruments



XTR115
XTR116

SBOS124A – JANUARY 2000 – REVISED NOVEMBER 2003

4-20mA CURRENT LOOP TRANSMITTERS

FEATURES

- LOW QUIESCENT CURRENT: 200µA
- 5V REGULATOR FOR EXTERNAL CIRCUITS
- V_{REF} FOR SENSOR EXCITATION:
  XTR115: 2.5V
  XTR116: 4.096V
- LOW SPAN ERROR: 0.05%
- LOW NONLINEARITY ERROR: 0.003%
- WIDE LOOP SUPPLY RANGE: 7.5V to 36V
- SO-8 PACKAGE

APPLICATIONS

- 2-WIRE, 4-20mA CURRENT LOOP TRANSMITTER
- SMART TRANSMITTER
- INDUSTRIAL PROCESS CONTROL
- TEST SYSTEMS
- COMPATIBLE WITH HART MODEM
- CURRENT AMPLIFIER
- VOLTAGE-TO-CURRENT AMPLIFIER

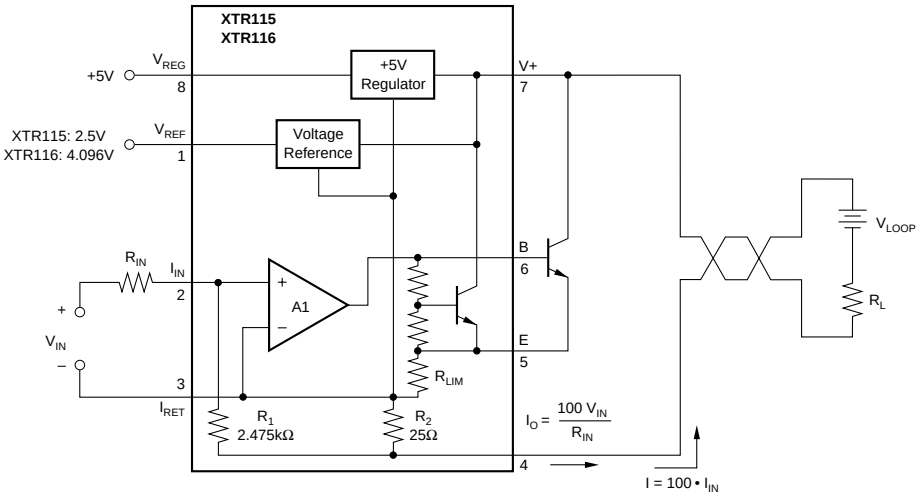
DESCRIPTION

The XTR115 and XTR116 are precision current output converters designed to transmit analog 4-to-20mA signals over an industry standard current loop. They provide accurate current scaling and output current limit functions.

The on-chip voltage regulator (5V) can be used to power external circuitry. A precision on-chip V_{REF} (2.5V for XTR115 and 4.096V for XTR116) can be used for offsetting or to excite transducers. A current return pin (I_{RET}) senses any current used in external circuitry to assure an accurate control of the output current.

The XTR115 is a fundamental building block of smart sensors using 4-to-20mA current transmission.

The XTR115 and XTR116 are specified for operation over the extended industrial temperature range, –40°C to +85°C.



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SPECIFICATIONS

At T_A = +25°C, V+ = 24V, R_{IN} = 20kΩ, and TIP29C external transistor, unless otherwise noted.

PARAMETER		CONDITIONS	XTR115U XTR116U MIN	XTR115U XTR116U TYP	XTR115U XTR116U MAX	XTR115UA XTR116UA MIN	XTR115UA XTR116UA TYP	XTR115UA XTR116UA MAX	UNITS
OUTPUT									
Output Current Equation	I_O			$I_O = I_{IN} \cdot 100$			*		
Output Current, Linear Range			0.25		25	*		*	mA
Over-Scale Limit	I_{LIM}			32			*		mA
Under-Scale Limit	I_{MIN}	I_{REG} = 0, I_{REF} = 0		0.2	0.25		*	*	mA
SPAN									
Span (Current Gain)	S			100			*		A/A
Error (1)		I_{IN} = 250µA to 25mA		±0.05	±0.2		*	±0.4	%
vs Temperature		T_A = –40°C to +85°C		±3	±20		*	*	ppm/°C
Nonlinearity		I_{IN} = 250µA to 25mA		±0.003	±0.01		*	±0.02	%
INPUT									
Offset Voltage (Op Amp)	V_{OS}	I_{IN} = 40µA		±100	±250		*	±500	µV
vs Temperature		T_A = –40°C to +85°C		±0.7	±3		*	±6	µV/°C
vs Supply Voltage, V+		V+ = 7.5V to 36V		±0.1	±2		*	*	µV/V
Bias Current	I_B			–35			*		nA
vs Temperature				150			*		pA/°C
Noise: 0.1Hz to 10Hz	e_n			0.6			*		µVp-p
DYNAMIC RESPONSE									
Small Signal Bandwidth		C_{LOOP} = 0, R_L = 0		380			*		kHz
Slew Rate				3.2			*		mA/µs
V_{REF} (2)									
XTR115				2.5			*		V
XTR116				4.096			*		V
Voltage Accuracy		I_{REF} = 0		±0.05	±0.25		*	±0.5	%
vs Temperature		T_A = –40°C to +85°C		±20	±35		*	±75	ppm/°C
vs Supply Voltage, V+		V+ = 7.5V to 36V		±1	±10		*	*	ppm/V
vs Load		I_{REF} = 0mA to 2.5mA		±100			*		ppm/mA
Noise: 0.1Hz to 10Hz				10			*		µVp-p
Short-Circuit Current				16			*		mA
V_{REG} (2)									
Voltage				5			*		V
Voltage Accuracy		I_{REG} = 0		±0.05	±0.1		*	*	V
vs Temperature		T_A = –40°C to +85°C		±0.1			*		mV/°C
vs Supply Voltage, V+		V+ = 7.5V to 36V		1			*		mV/V
vs Output Current				See Typical Curves					
Short-Circuit Current				12			*		mA
POWER SUPPLY	V+								
Specified				+24			*		V
Voltage Range			+7.5		+36	*		*	V
Quiescent Current				200	250		*	*	µA
Over Temperature, –40°C to +85°C				240	300		*	*	µA
TEMPERATURE RANGE									
Specification			–40		+85	*		*	°C
Operating			–55		+125	*		*	°C
Storage			–55		+125	*		*	°C
Thermal Resistance	θ_{JA}			150			*		°C/W

* Specifications the same as XTR115U and XTR116U.

NOTES: (1) Does not include initial error or TCR of R_{IN}. (2) Voltage measured with respect to I_{RET} pin.

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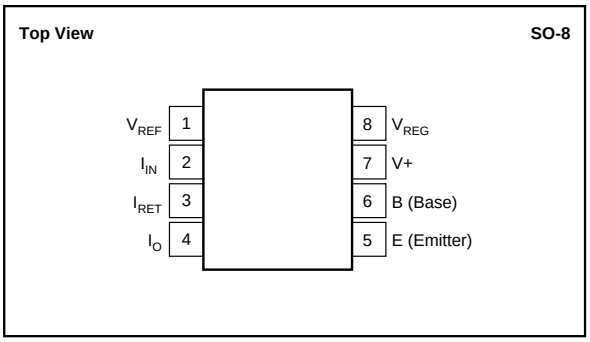
PIN CONFIGURATION



PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS(1)

Power Supply, V+ (referenced to I_O pin)	40V
Input Voltage (referenced to I_{RET} pin)	0V to V+
Output Current Limit	Continuous
V_{REG}, Short-Circuit	Continuous
V_{REF}, Short-Circuit	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature Range	–55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+165°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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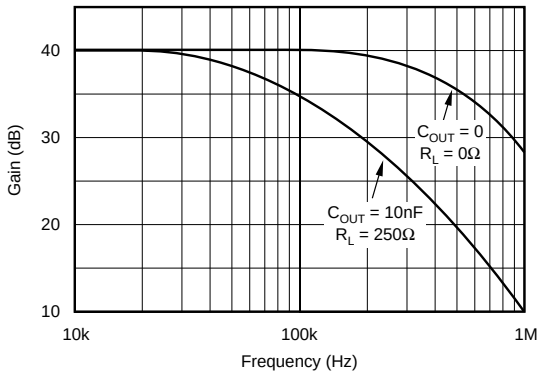
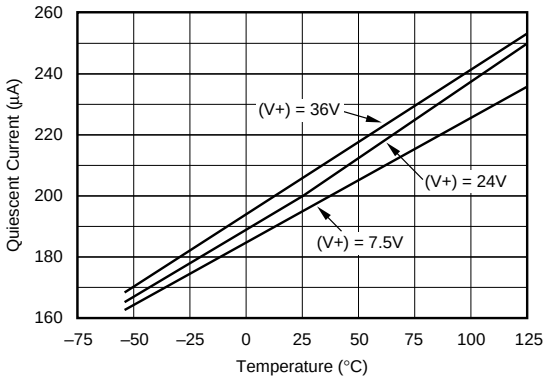
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V+ = 24V, R_{IN} = 20kΩ, and TIP29C external transistor, unless otherwise noted.

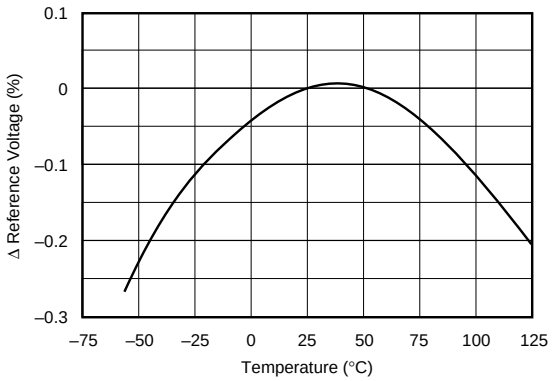
CURRENT GAIN vs FREQUENCY



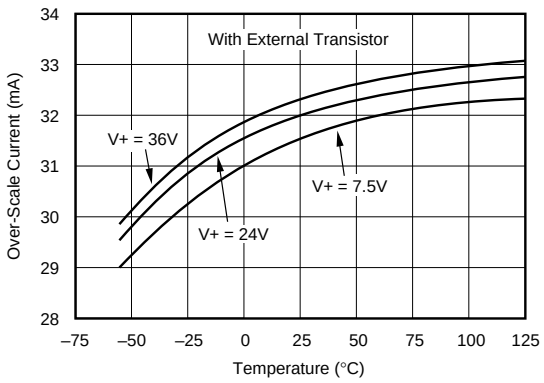
QUIESCENT CURRENT vs TEMPERATURE



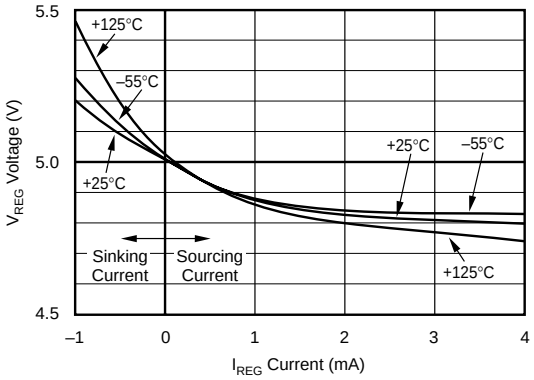
REFERENCE VOLTAGE vs TEMPERATURE



OVER-SCALE CURRENT vs TEMPERATURE



V_{REG} VOLTAGE vs V_{REG} CURRENT



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APPLICATIONS INFORMATION

The XTR115 and XTR116 are identical devices except for the reference voltage output, pin 1. This voltage is available for external circuitry and is not used internally. Further discussions that apply to both devices will refer to the "XTR115/6."

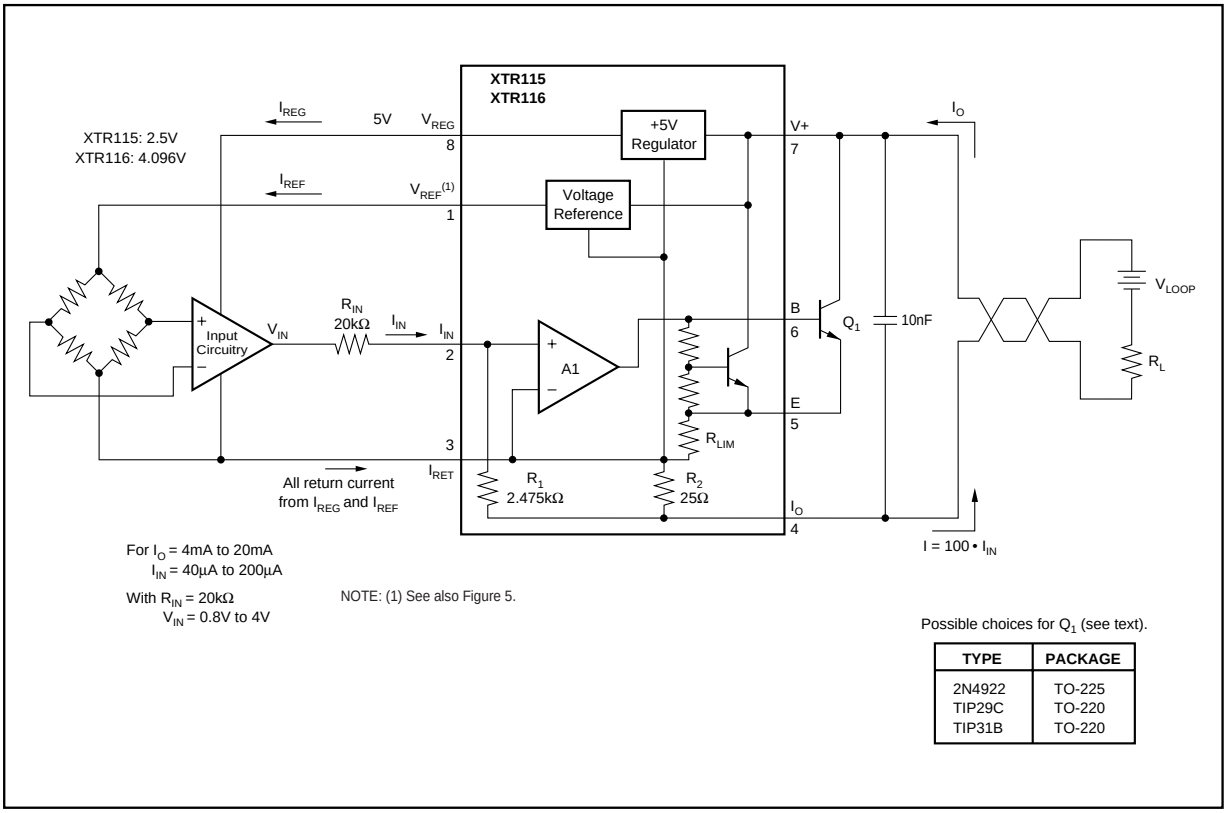
Figure 1 shows basic circuit connections with representative simplified input circuitry. The XTR115/6 is a two-wire current transmitter. Its input signal (pin 2) controls the output current. A portion of this current flows into the V+ power supply, pin 7. The remaining current flows in Q1. External input circuitry connected to the XTR115/6 can be powered from V_{REG} or V_{REF}. Current drawn from these terminals must be returned to I_{RET}, pin 3. This I_{RET} pin is a "local ground" for input circuitry driving the XTR115/6.

The XTR115/6 is a current-input device with a gain of 100. A current flowing into pin 2 produces $I_O = 100 \cdot I_{IN}$. The input voltage at the I_{IN} pin is zero (referred to the I_{RET} pin). A voltage input is created with an external input resistor, as shown. Common full-scale input voltages range from 1V and upward. Full-scale inputs greater than 0.5V are recommend to minimize the effect of offset voltage and drift of A1.

EXTERNAL TRANSISTOR

The external transistor, Q1, conducts the majority of the full-scale output current. Power dissipation in this transistor can approach 0.8W with high loop voltage (40V) and 20mA output current. The XTR115/6 is designed to use an external transistor to avoid on-chip thermal-induced errors. Heat produced by Q1 will still cause ambient temperature changes that can affect the XTR115/6. To minimize these effects, locate Q1 away from sensitive analog circuitry, including XTR115/6. Mount Q1 so that heat is conducted to the outside of the transducer housing.

The XTR115/6 is designed to use virtually any NPN transistor with sufficient voltage, current and power rating. Case style and thermal mounting considerations often influence the choice for any given application. Several possible choices are listed in Figure 1. A MOSFET transistor will not improve the accuracy of the XTR115/6 and is not recommended.



TYPE	PACKAGE
2N4922	TO-225
TIP29C	TO-220
TIP31B	TO-220

FIGURE 1. Basic Circuit Connections.

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MINIMUM-SCALE CURRENT

The quiescent current of the XTR115/6 (typically 200µA) is the lower limit of its output current. Zero input current (I_{IN} = 0) will produce an I_O equal to the quiescent current. Output current will not begin to increase until $I_{IN} > I_Q/100$. Current drawn from V_{REF} or V_{REG} will add to this minimum output current. This means that more than 3.7mA is available to power external circuitry while still allowing the output current to go below 4mA.

OFFSETTING THE INPUT

A low scale of 4mA is produced by creating a 40µA input current. This can be created with the proper value resistor from V_{REF} (Figure 2), or by generating offset in the input drive circuitry.

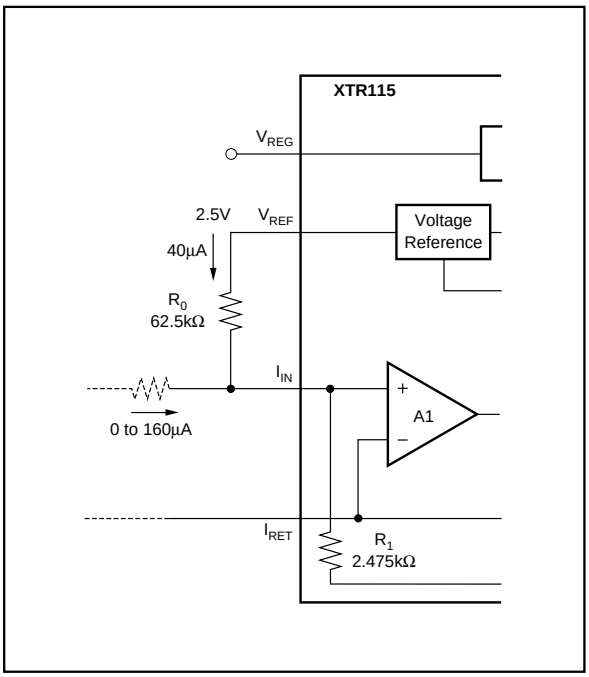

FIGURE 2. Creating Low-Scale Offset.

MAXIMUM OUTPUT CURRENT

The XTR115/6 provides accurate, linear output up to 25mA. Internal circuitry limits the output current to approximately 32mA to protect the transmitter and loop power/measurement circuitry.

It is possible to extend the output current range of the XTR115/6 by connecting an external resistor from pin 3 to pin 5, to change the current limit value. Since all output current must flow through internal resistors, it is possible to damage with excessive current. Output currents greater than 45mA may cause permanent damage.

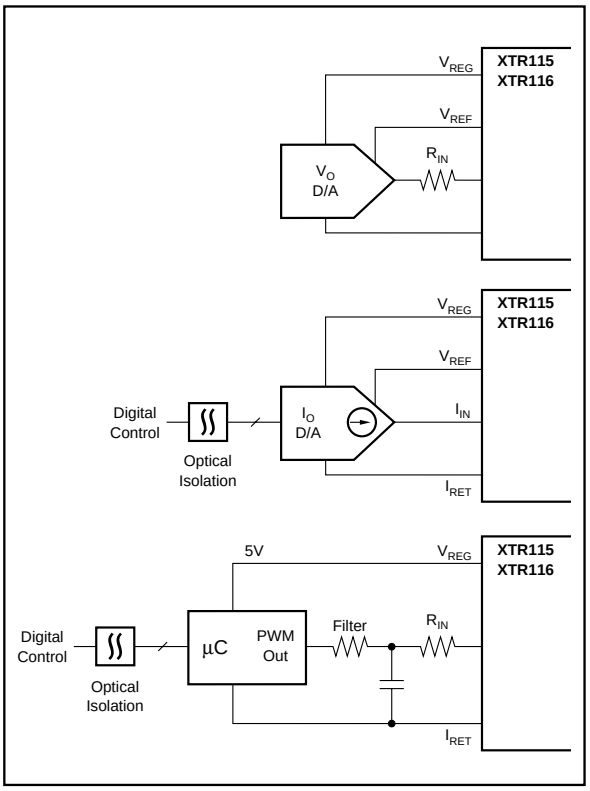

FIGURE 3. Digital Control Methods.

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REVERSE-VOLTAGE PROTECTION

The XTR115/6 low compliance voltage rating (7.5V) permits the use of various voltage protection methods without compromising operating range. Figure 4 shows a diode bridge circuit which allows normal operation even when the voltage connection lines are reversed. The bridge causes a two diode drop (approximately 1.4V) loss in loop supply voltage. This results in a compliance voltage of approximately 9V—satisfactory for most applications. A diode can be inserted in series with the loop supply voltage and the V+ pin to protect against reverse output connection lines with only a 0.7V loss in loop supply voltage.

OVER-VOLTAGE SURGE PROTECTION

Remote connections to current transmitters can sometimes be subjected to voltage surges. It is prudent to limit the maximum surge voltage applied to the XTR115/6 to as low as practical. Various zener diode and surge clamping diodes are specially designed for this purpose. Select a clamp diode with as low a voltage rating as possible for best protection. For example, a 36V protection diode will assure proper transmitter operation at normal loop voltages, yet will provide an appropriate level of protection against voltage surges. Characterization tests on several production lots showed no damage with loop supply voltages up to 65V.

Most surge protection zener diodes have a diode characteristic in the forward direction that will conduct excessive current, possibly damaging receiving-side circuitry if the loop connections are reversed. If a surge protection diode is used, a series diode or diode bridge should be used for protection against reversed connections.

RADIO FREQUENCY INTERFERENCE

The long wire lengths of current loops invite radio frequency interference. RF can be rectified by the input circuitry of the XTR115/6 or preceding circuitry. This generally appears as an unstable output current that varies with the position of loop supply or input wiring.

Interference may also enter at the input terminals. For integrated transmitter assemblies with short connection to the sensor, the interference more likely comes from the current loop connections.

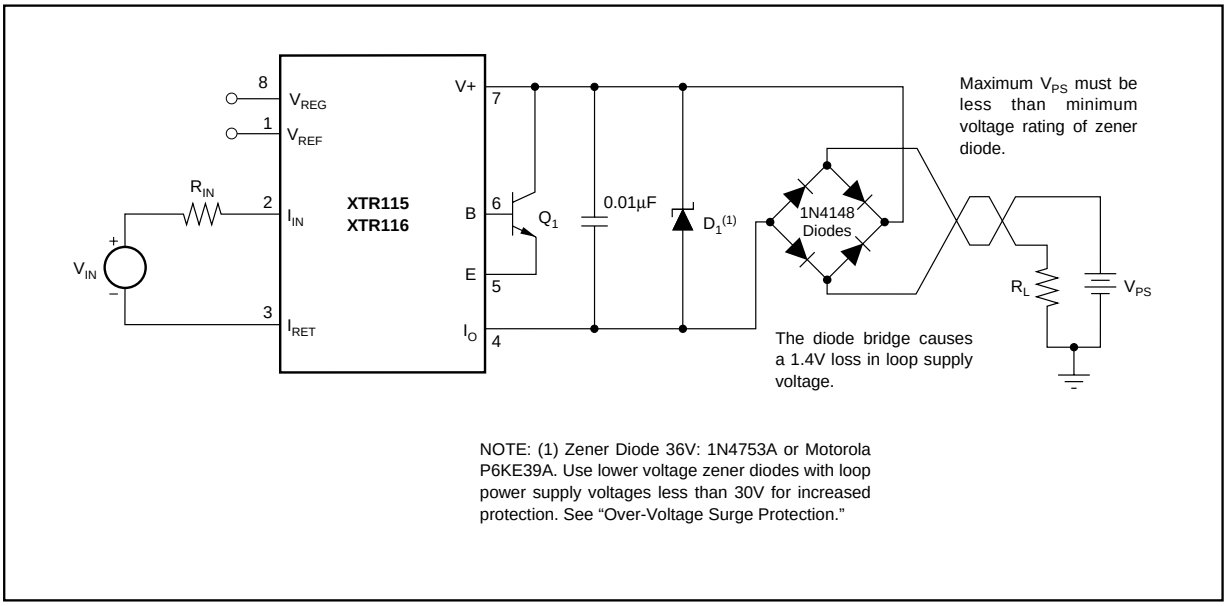

FIGURE 4. Reverse Voltage Operation and Over-Voltage Surge Protection.

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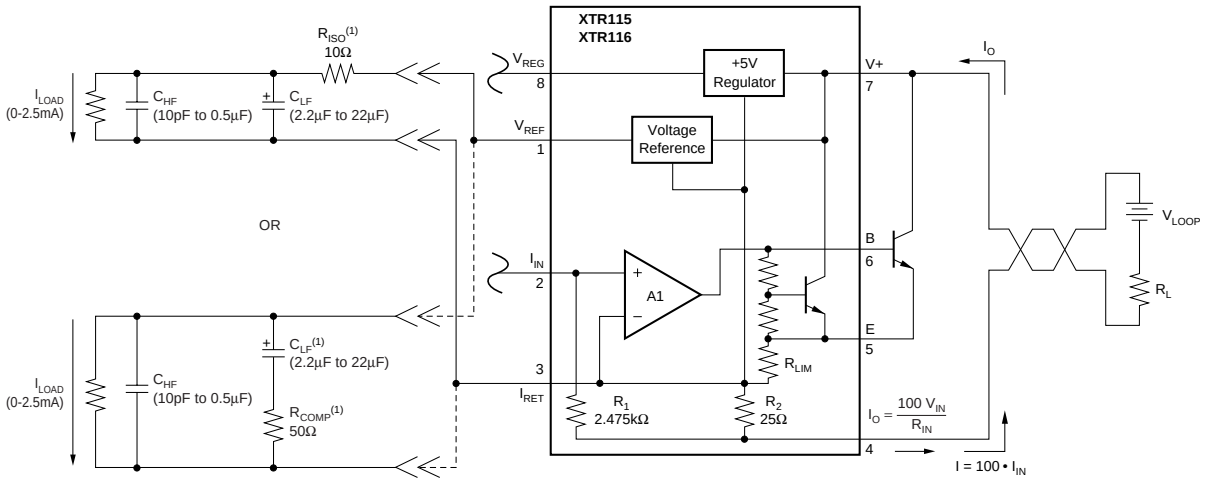
If capacitive loading must be placed on the V_{REF} pin, one of the compensation schemes shown below must be used to ensure stable operation. Values of capacitance must remain within the given ranges.



NOTE: (1) Required compensation components.

FIGURE 5. Stable Operation with Capacitive Load on V_{REF}.

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PACKAGE OPTION ADDENDUM

25-Oct-2016

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XTR115U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		XTR 115U	Samples
XTR115U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		XTR 115U	Samples
XTR115U/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		XTR 115U	Samples
XTR115UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		XTR 115U A	Samples
XTR115UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		XTR 115U A	Samples
XTR115UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		XTR 115U A	Samples
XTR115UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		XTR 115U	Samples
XTR116U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		XTR 116U	Samples
XTR116U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		XTR 116U	Samples
XTR116U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		XTR 116U	Samples
XTR116UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		XTR 116U A	Samples
XTR116UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		XTR 116U A	Samples
XTR116UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		XTR 116U A	Samples
XTR116UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		XTR 116U A	Samples

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PACKAGE OPTION ADDENDUM

25-Oct-2016

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XTR116UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		XTR 116U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

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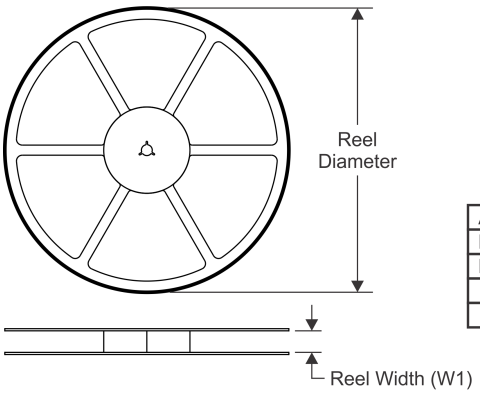
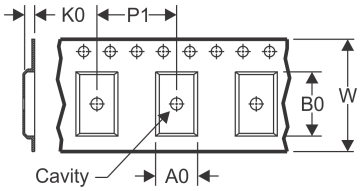
TAPE AND REEL INFORMATION

REEL DIMENSIONS

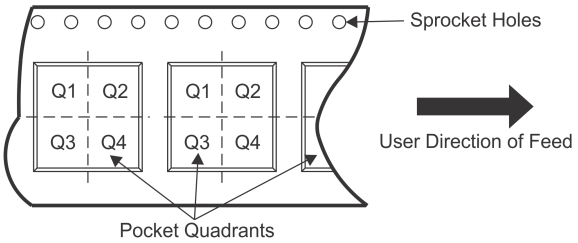


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XTR115U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
XTR115UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
XTR116U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

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PACKAGE MATERIALS INFORMATION

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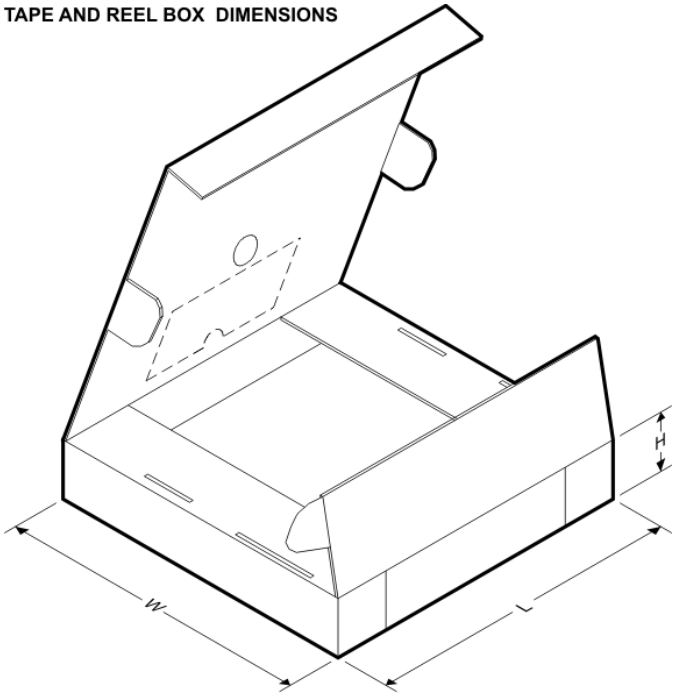
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XTR115U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
XTR115UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
XTR116U/2K5	SOIC	D	8	2500	367.0	367.0	35.0

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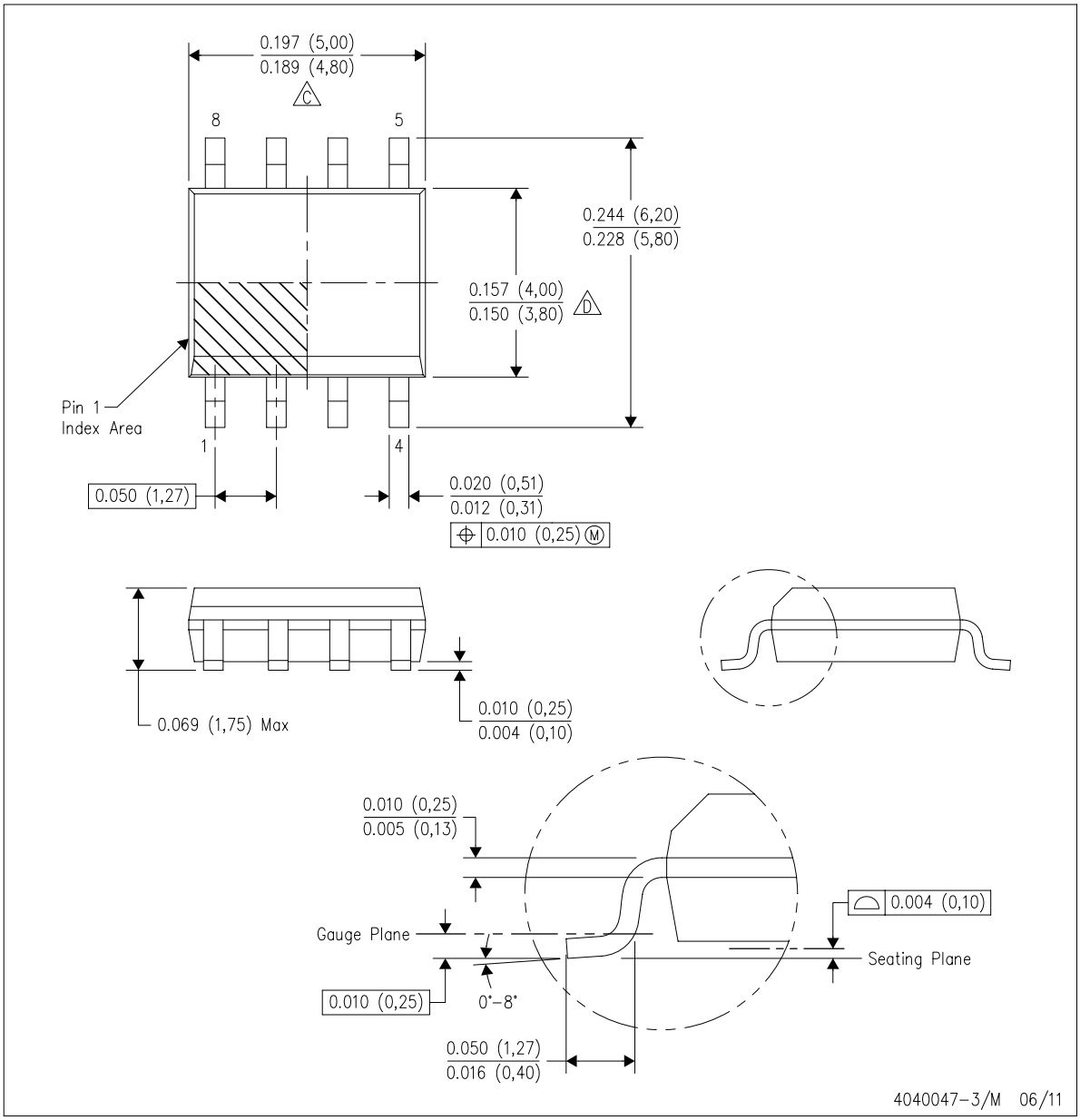
MECHANICAL DATA

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AA.

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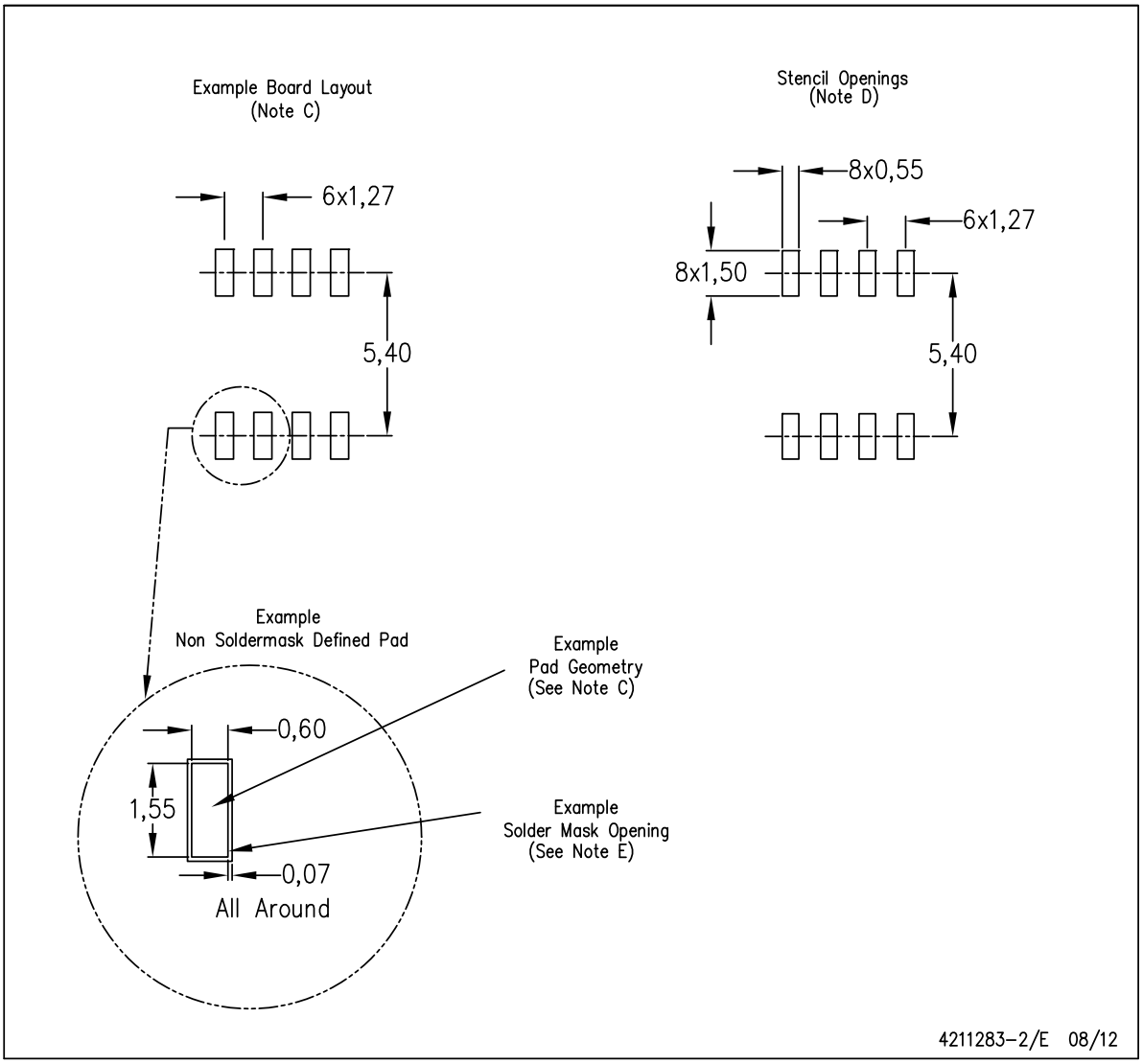
LAND PATTERN DATA

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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