Quad 64-/256-Position I²C Nonvolatile Memory Digital Potentiometers

Data Sheet **AD5253/AD5254**

FEATURES

AD5253: quad 64-position resolution
AD5254: quad 256-position resolution
1 kΩ, 10 kΩ, 50 kΩ, 100 kΩ
Nonvolatile memory[1] stores wiper settings w/write protection
Power-on refreshed to EEMEM settings in 300 µs typ
EEMEM rewrite time = 540 µs typ
Resistance tolerance stored in nonvolatile memory
12 extra bytes in EEMEM for user-defined information
I²C-compatible serial interface
Direct read/write access of RDAC[2] and EEMEM registers
Predefined linear increment/decrement commands
Predefined ±6 dB step change commands
Synchronous or asynchronous quad-channel update
Wiper setting readback
4 MHz bandwidth—1 kΩ version
Single supply 2.7 V to 5.5 V
Dual supply ±2.25 V to ±2.75 V
2 slave address-decoding bits allow operation of 4 devices
100-year typical data retention, T_A = 55°C
Operating temperature: –40°C to +105°C

APPLICATIONS

Mechanical potentiometer replacement
Low resolution DAC replacement
RGB LED backlight control
White LED brightness adjustment
RF base station power amp bias control
Programmable gain and offset control
Programmable attenuators
Programmable voltage-to-current conversion
Programmable power supply
Programmable filters
Sensor calibrations

GENERAL DESCRIPTION

The AD5253/AD5254 are quad-channel, I²C®, nonvolatile mem-ory, digitally controlled potentiometers with 64/256 positions, respectively. These devices perform the same electronic adjust-ment functions as mechanical potentiometers, trimmers, and variable resistors.

The parts' versatile programmability allows multiple modes of operation, including read/write access in the RDAC and EEMEM registers, increment/decrement of resistance, resistance changes in ±6 dB scales, wiper setting readback, and extra EEMEM for storing user-defined information, such as memory data for other components, look-up table, or system identification information.

FUNCTIONAL BLOCK DIAGRAM

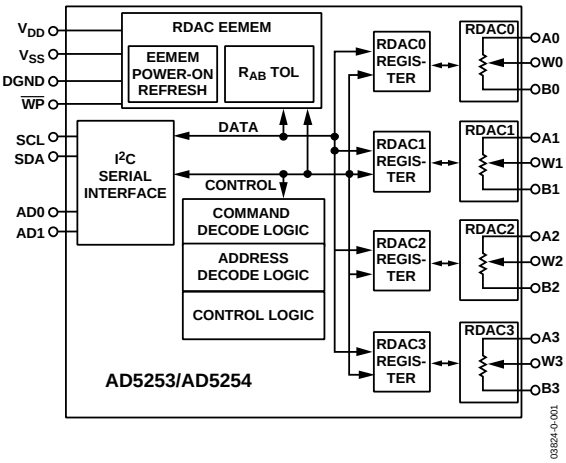

Figure 1.

The AD5253/AD5254 allow the host I²C controllers to write any of the 64-/256-step wiper settings in the RDAC registers and store them in the EEMEM. Once the settings are stored, they are restored automatically to the RDAC registers at system power-on; the settings can also be restored dynamically.

The AD5253/AD5254 provide additional increment, decrement, +6 dB step change, and –6 dB step change in synchronous or asynchronous channel update mode. The increment and decrement functions allow stepwise linear adjustments, with a ± 6 dB step change equivalent to doubling or halving the RDAC wiper setting. These functions are useful for steep-slope, nonlinear adjustments, such as white LED brightness and audio volume control.

The AD5253/AD5254 have a patented resistance-tolerance storing function that allows the user to access the EEMEM and obtain the absolute end-to-end resistance values of the RDACs for precision applications.

The AD5253/AD5254 are available in TSSOP-20 packages in 1 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ options. All parts are guaranteed to operate over the –40°C to +105°C extended industrial temperature range.

[1]The terms *nonvolatile memory* and *EEMEM* are used interchangeably.
[2]The terms *digital potentiometer* and *RDAC* are used interchangeably.

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REVISION HISTORY

9/12—Rev. B to Rev. C

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10/09—Rev. A to Rev. B

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5/03—Revision 0: Initial Version

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ELECTRICAL CHARACTERISTICS

1 kΩ VERSION

V_{DD} = +3 V ± 10% or +5 V ± 10%, V_{SS} = 0 V or V_{DD}/V_{SS} = ±2.5 V ± 10%, $V_A = V_{DD}$, V_B = 0 V, –40°C < T_A < +105°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resolution	N	AD5253			6	Bits
		AD5254			8	Bits
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, R_{WA} = NC, V_{DD} = 5.5 V, AD5253	–0.5	±0.2	+0.5	LSB
		R_{WB}, R_{WA} = NC, V_{DD} = 5.5 V, AD5254	–1.00	±0.25	+1.00	LSB
		R_{WB}, R_{WA} = NC, V_{DD} = 2.7 V, AD5253	–0.75	±0.30	+0.75	LSB
		R_{WB}, R_{WA} = NC, V_{DD} = 2.7 V, AD5254	–1.5	±0.3	+1.5	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, R_{WA} = NC, V_{DD} = 5.5 V, AD5253	–0.5	±0.2	+0.5	LSB
		R_{WB}, R_{WA} = NC, V_{DD} = 5.5 V, AD5254	–2.0	±0.5	+2.0	LSB
		R_{WB}, R_{WA} = NC, V_{DD} = 2.7 V, AD5253	–1.0	+2.5	+4.0	LSB
		R_{WB}, R_{WA} = NC, V_{DD} = 2.7 V, AD5254	–2	+9	+14	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$	T_A = 25°C	–30		+30	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB}) \times 10^6/\Delta T$			650		ppm/°C
Wiper Resistance	R_W	I_W = 1 V/R, V_{DD} = 5 V		75	130	Ω
		I_W = 1 V/R, V_{DD} = 3 V		200	300	Ω
Channel-Resistance Matching	$\Delta R_{AB1}/\Delta R_{AB2}$			0.15		%
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Differential Nonlinearity[3]	DNL	AD5253	–0.5	±0.1	+0.5	LSB
		AD5254	–1.00	±0.25	+1.00	LSB
Integral Nonlinearity[3]	INL	AD5253	–0.5	±0.2	+0.5	LSB
		AD5254	–2.0	±0.5	+2.0	LSB
Voltage Divider Tempco	$(\Delta V_W/V_W) \times 10^6/\Delta T$	Code = half scale		25		ppm/°C
Full-Scale Error	V_{WFSE}	Code = full scale, V_{DD} = 5.5 V, AD5253	–5	–3	0	LSB
		Code = full scale, V_{DD} = 5.5 V, AD5254	–16	–11	0	LSB
		Code = full scale, V_{DD} = 2.7 V, AD5253	–6	–4	0	LSB
		Code = full scale, V_{DD} = 2.7 V, AD5254	–23	–16	0	LSB
Zero-Scale Error	V_{WZSE}	Code = zero scale, V_{DD} = 5.5 V, AD5253	0	3	5	LSB
		Code = zero scale, V_{DD} = 5.5 V, AD5254	0	11	16	LSB
		Code = zero scale, V_{DD} = 2.7 V, AD5253	0	4	6	LSB
		Code = zero scale, V_{DD} = 2.7 V, AD5254	0	15	20	LSB
RESISTOR TERMINALS						
Voltage Range[4]	V_A, V_B, V_W		V_{SS}		V_{DD}	V
Capacitance[5] A, B	C_A, C_B	f = 1 kHz, measured to GND, code = half scale		85		pF
Capacitance[5] W	C_W	f = 1 kHz, measured to GND, code = half scale		95		pF
Common-Mode Leakage Current	I_{CM}	$V_A = V_B = V_{DD}/2$		0.01	1.00	µA

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AD5253/AD5254 Data Sheet

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V, V_{SS} = 0 V	2.4			V
		V_{DD}/V_{SS} = +2.7 V/0 V or V_{DD}/V_{SS} = ±2.5 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 5 V, V_{SS} = 0 V			0.8	V
		V_{DD}/V_{SS} = +2.7 V/0 V or V_{DD}/V_{SS} = ±2.5 V			0.6	V
Output Logic High (SDA)	V_{OH}	$R_{PULL-UP}$ = 2.2 kΩ to V_{DD} = 5 V, V_{SS} = 0 V	4.9			V
Output Logic Low (SDA)	V_{OL}	$R_{PULL-UP}$ = 2.2 kΩ to V_{DD} = 5 V, V_{SS} = 0 V			0.4	V
$\overline{WP}$ Leakage Current	I_{WP}	$\overline{WP}$ = V_{DD}			8	µA
A0 Leakage Current	I_{A0}	A0 = GND			3	µA
Input Leakage Current (Other than $\overline{WP}$ and A0)	I_I	V_{IN} = 0 V or V_{DD}			±1	µA
Input Capacitance[5]	C_I			5		pF
POWER SUPPLIES						
Single-Supply Power Range	V_{DD}	V_{SS} = 0 V	2.7		5.5	V
Dual-Supply Power Range	V_{DD}/V_{SS}		±2.25		±2.75	V
Positive Supply Current	I_{DD}	V_{IH} = V_{DD} or V_{IL} = GND		5	15	µA
Negative Supply Current	I_{SS}	V_{IH} = V_{DD} or V_{IL} = GND, V_{DD} = 2.5 V, V_{SS} = −2.5 V		−5	−15	µA
EEMEM Data Storing Mode Current	I_{DD_STORE}	V_{IH} = V_{DD} or V_{IL} = GND		35		mA
EEMEM Data Restoring Mode Current[6]	$I_{DD_RESTORE}$	V_{IH} = V_{DD} or V_{IL} = GND		2.5		mA
Power Dissipation[7]	P_{DISS}	V_{IH} = V_{DD} = 5 V or V_{IL} = GND			0.075	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = 5 V ± 10%	−0.025	+0.010	+0.025	%/%
		ΔV_{DD} = 3 V ± 10%	−0.04	+0.02	+0.04	%/%
DYNAMIC CHARACTERISTICS[5, 8]						
Bandwidth −3 dB	BW	R_{AB} = 1 kΩ		4		MHz
Total Harmonic Distortion	THD	V_A =1 V rms, V_B = 0 V, f = 1 kHz		0.05		%
V_W Settling Time	t_S	V_A = V_{DD}, V_B = 0 V		0.2		µs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 500 Ω, f = 1 kHz (thermal noise only)		3		nV/√Hz
Digital Crosstalk	C_T	V_A = V_{DD}, V_B = 0 V, measure V_W with adjacent RDAC making full-scale change		−80		dB
Analog Coupling	C_{AT}	Signal input at A0 and measure the output at W1, f = 1 kHz		−72		dB

[1] Typical values represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum and minimum resistance wiper positions. R-DNL is the relative step change from an ideal value measured between successive tap positions. Parts are guaranteed monotonic, except R-DNL of AD5254 1 kΩ version at V_{DD} = 2.7 V, I_W = V_{DD}/R for both V_{DD} = 3 V and V_{DD} = 5 V.
[3] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output digital-to-analog converter. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[4] Resistor Terminal A, Terminal B, and Terminal W have no limitations on polarity with respect to each other.
[5] Guaranteed by design and not subject to production test.
[6] Command 0 NOP should be activated after Command 1 to minimize $I_{DD_RESTORE}$ current consumption.
[7] P_{DISS} is calculated from $I_{DD} \times V_{DD}$ = 5 V.
[8] All dynamic characteristics use V_{DD} = 5 V.

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10 kΩ, 50 kΩ, 100 kΩ VERSIONS

V_{DD} = +3 V ± 10% or +5 V ± 10%, V_{SS} = 0 V or V_{DD}/V_{SS} = ±2.5 V ± 10%, $V_A = V_{DD}$, V_B = 0 V, –40°C < T_A < +105°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resolution	N	AD5253/AD5254			6/8	Bits
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, R_{WA} = NC, AD5253	–0.75	±0.10	+0.75	LSB
		R_{WB}, R_{WA} = NC, AD5254	–1.00	±0.25	+1.00	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, R_{WA} = NC, AD5253	–0.75	±0.25	+0.75	LSB
		R_{WB}, R_{WA} = NC, AD5254	–2.5	±1.0	+2.5	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$	T_A = 25°C	–20		+20	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB}) \times 10^6/\Delta T$			650		ppm/°C
Wiper Resistance	R_W	I_W = 1 V/R, V_{DD} = 5 V		75	130	Ω
		I_W = 1 V/R, V_{DD} = 3 V		200	300	Ω
Channel-Resistance Matching	$\Delta R_{AB1}/\Delta R_{AB2}$	R_{AB} = 10 kΩ, 50 kΩ		0.15		%
		R_{AB} = 100 kΩ		0.05		%
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Differential Nonlinearity[3]	DNL	AD5253	–0.5	±0.1	+0.5	LSB
		AD5254	–1.0	±0.3	+1.0	LSB
Integral Nonlinearity[3]	INL	AD5253	–0.50	±0.15	+0.50	LSB
		AD5254	–1.5	±0.5	+1.5	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W) \times 10^6/\Delta T$	Code = half scale		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = full scale, AD5253	–1.0	–0.3	0	LSB
		Code = full scale, AD5254	–3	–1	0	LSB
Zero-Scale Error	V_{WZSE}	Code = zero scale, AD5253	0	0.3	1.0	LSB
		Code = zero scale, AD5254	0	1.2	3.0	LSB
RESISTOR TERMINALS						
Voltage Range[4]	V_A, V_B, V_W		V_{SS}		V_{DD}	V
Capacitance[5] A, B	C_A, C_B	f = 1 kHz, measured to GND, code = half scale		85		pF
Capacitance[5] W	C_W	f = 1 kHz, measured to GND, code = half scale		95		pF
Common-Mode Leakage Current	I_{CM}	$V_A = V_B = V_{DD}/2$		0.01	1	µA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V, V_{SS} = 0 V	2.4			V
		V_{DD}/V_{SS} = +2.7 V/0 V or V_{DD}/V_{SS} = ±2.5 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 5 V, V_{SS} = 0 V			0.8	V
		V_{DD}/V_{SS} = +2.7 V/0 V or V_{DD}/V_{SS} = ±2.5 V			0.6	V
Output Logic High (SDA)	V_{OH}	$R_{PULL-UP}$ = 2.2 kΩ to V_{DD} = 5 V, V_{SS} = 0 V	4.9			V
Output Logic Low (SDA)	V_{OL}	$R_{PULL-UP}$ = 2.2 kΩ to V_{DD} = 5 V, V_{SS} = 0 V			0.4	V
$\overline{WP}$ Leakage Current	I_{WP}	$\overline{WP} = V_{DD}$			8	µA
A0 Leakage Current	I_{A0}	A0 = GND			3	µA
Input Leakage Current (Other than $\overline{WP}$ and A0)	I_I	V_{IN} = 0 V or V_{DD}			±1	µA
Input Capacitance[5]	C_I			5		pF

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Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
POWER SUPPLIES						
Single-Supply Power Range	V_{DD}	V_{SS} = 0 V	2.7		5.5	V
Dual-Supply Power Range	V_{DD}/V_{SS}		±2.25		±2.75	V
Positive Supply Current	I_{DD}	$V_{IH} = V_{DD}$ or V_{IL} = GND		5	15	µA
Negative Supply Current	I_{SS}	$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{DD} = 2.5 V, V_{SS} = −2.5 V		−5	−15	µA
EEMEM Data Storing Mode Current	I_{DD_STORE}	$V_{IH} = V_{DD}$ or V_{IL} = GND, T_A = 0°C to 105°C		35		mA
EEMEM Data Restoring Mode Current[6]	$I_{DD_RESTORE}$	$V_{IH} = V_{DD}$ or V_{IL} = GND, T_A = 0°C to 105°C		2.5		mA
Power Dissipation[7]	P_{DISS}	$V_{IH} = V_{DD}$ = 5 V or V_{IL} = GND			0.075	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = 5 V ± 10%	−0.005	+0.002	+0.005	%/%
		ΔV_{DD} = 3 V ± 10%	−0.010	+0.002	+0.010	%/%
DYNAMIC CHARACTERISTICS[5, 8]						
−3 dB Bandwidth	BW	R_{AB} = 10 kΩ/50 kΩ/100 kΩ		400/80/40		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.05		%
V_W Settling Time	t_S	$V_A = V_{DD}$, V_B = 0 V, R_{AB} = 10 kΩ/50 kΩ/100 kΩ		1.5/7/14		µs
Resistor Noise Voltage	e_{N_WB}	R_{AB} = 10 kΩ/50 kΩ/100 kΩ, code = midscale, f = 1 kHz (thermal noise only)		9/20/29		nV/√Hz
Digital Crosstalk	C_T	$V_A = V_{DD}$, V_B = 0 V, measure V_W with adjacent RDAC making full-scale change		−80		dB
Analog Coupling	C_{AT}	Signal input at A0 and measure output at W1, f = 1 kHz		−72		dB

[1] Typical values represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum and minimum resistance wiper positions. R-DNL is the relative step change from an ideal value measured between successive tap positions. Parts are guaranteed monotonic, except R-DNL of AD5254 1 kΩ version at V_{DD} = 2.7 V, $I_W = V_{DD}/R$ for both V_{DD} = 3 V and V_{DD} = 5 V.
[3] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider, similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[4] Resistor Terminal A, Terminal B, and Terminal W have no limitations on polarity with respect to each other.
[5] Guaranteed by design and not subject to production test.
[6] Command 0 NOP should be activated after Command 1 to minimize $I_{DD_RESTORE}$ current consumption.
[7] P_{DISS} is calculated from $I_{DD} \times V_{DD}$ = 5 V.
[8] All dynamic characteristics use V_{DD} = 5 V.

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INTERFACE TIMING CHARACTERISTICS

All input control voltages are specified with $t_R = t_F = 2.5$ ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V. Switching characteristics are measured using both $V_{DD} = 3$ V and 5 V.

Table 3.

Parameter[1]	Symbol	Conditions	Min	Typ[2]	Max	Unit
INTERFACE TIMING						
SCL Clock Frequency	f_{SCL}				400	kHz
t_{BUF} Bus-Free Time Between Stop and Start	t_1		1.3			µs
$t_{HD;STA}$ Hold Time (Repeated Start)	t_2	After this period, the first clock pulse is generated.	0.6			µs
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6			µs
$t_{SU;STA}$ Set-up Time for Start Condition	t_5		0.6			µs
$t_{HD;DAT}$ Data Hold Time	t_6		0		0.9	µs
$t_{SU;DAT}$ Data Set-up Time	t_7		100			ns
t_F Fall Time of Both SDA and SCL Signals	t_8				300	ns
t_R Rise Time of Both SDA and SCL Signals	t_9				300	ns
$t_{SU;STO}$ Set-up Time for Stop Condition	t_{10}		0.6			µs
EEMEM Data Storing Time	t_{EEMEM_STORE}			26		ms
EEMEM Data Restoring Time at Power-On[3]	$t_{EEMEM_RESTORE1}$	V_{DD} rise time dependent. Measure without decoupling capacitors at V_{DD} and V_{SS}.		300		µs
EEMEM Data Restoring Time upon Restore Command or Reset Operation[3]	$t_{EEMEM_RESTORE2}$	$V_{DD} = 5$ V.		300		µs
EEMEM Data Rewritable Time[4]	$t_{EEMEM_REWRITE}$			540		µs
FLASH/EE MEMORY RELIABILITY						
Endurance[5]			100			K cycles
Data Retention[6, 7]				100		Years

[1] See Figure 23 for location of measured values.
[2] Typical values represent average readings at 25°C and $V_{DD} = 5$ V.
[3] During power-up, all outputs are preset to midscale before restoring the EEMEM contents. RDAC0 has the shortest EEMEM restore time, whereas RDAC3 has the longest.
[4] Delay time after power-on or reset before new EEMEM data to be written.
[5] Endurance is qualified to 100,000 cycles per JEDEC Std. 22 Method A117 and measured at –40°C, +25°C, and +105°C; typical endurance at +25°C is 700,000 cycles.
[6] Retention lifetime equivalent at junction temperature $T_J = 55$°C per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature.
[7] When the part is not in operation, the SDA and SCL pins should be pulled high. When these pins are pulled low, the I^2C interface at these pins conducts a current of about 0.8 mA at $V_{DD} = 5.5$ V and 0.2 mA at $V_{DD} = 2.7$ V.

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V, +7 V
V_{SS} to GND	+0.3 V, −7 V
V_{DD} to V_{SS}	7 V
V_A, V_B, V_W to GND	V_{SS}, V_{DD}
Maximum Current	
I_{WB}, I_{WA} Pulsed	±20 mA
I_{WB} Continuous (R_{WB} ≤ 1 kΩ, A Open)[1]	±5 mA
I_{WA} Continuous (R_{WA} ≤ 1 kΩ, B Open)[1]	±5 mA
I_{AB} Continuous (R_{AB} = 1 kΩ/10 kΩ/50 kΩ/100 kΩ)[1]	±5 mA/±500 µA/ ±100 µA/±50 µA
Digital Inputs and Output Voltage to GND	0 V, 7 V
Operating Temperature Range	−40°C to +105°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
TSSOP-20 Thermal Resistance[2] θ_{JA}	143°C/W

[1] Maximum terminal current is bound by the maximum applied voltage across any two of the A, B, and W terminals at a given resistance, the maximum current handling of the switches, and the maximum power dissipation of the package. V_{DD} = 5 V.
[2] Package power dissipation = $(T_{JMAX} - T_A)/\theta_{JA}$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

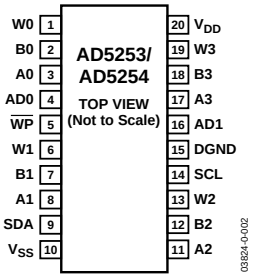

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	W0	Wiper Terminal of RDAC0. $V_{SS} \le V_{W0} \le V_{DD}$.
2	B0	B Terminal of RDAC0. $V_{SS} \le V_{B0} \le V_{DD}$.
3	A0	A Terminal of RDAC0. $V_{SS} \le V_{A0} \le V_{DD}$.
4	AD0	I^2C Device Address 0. AD0 and AD1 allow four AD5253/AD5254 devices to be addressed.
5	$\overline{WP}$	Write Protect, Active Low. $V_{WP} \le V_{DD} + 0.3$ V.
6	W1	Wiper Terminal of RDAC1. $V_{SS} \le V_{W1} \le V_{DD}$.
7	B1	B Terminal of RDAC1. $V_{SS} \le V_{B1} \le V_{DD}$.
8	A1	A Terminal of RDAC1. $V_{SS} \le V_{A1} \le V_{DD}$.
9	SDA	Serial Data Input/Output Pin. Shifts in one bit at a time upon positive clock edges. MSB loaded first. Open-drain MOSFET requires pull-up resistor.
10	V_{SS}	Negative Supply. Connect to 0 V for single supply or −2.7 V for dual supply, where $V_{DD} - V_{SS} \le +5.5$ V. If V_{SS} is used rather than grounded in dual supply, V_{SS} must be able to sink 35 mA for 26 ms when storing data to EEMEM.
11	A2	A Terminal of RDAC2. $V_{SS} \le V_{A2} \le V_{DD}$.
12	B2	B Terminal of RDAC2. $V_{SS} \le V_{B2} \le V_{DD}$.
13	W2	Wiper Terminal of RDAC2. $V_{SS} \le V_{W2} \le V_{DD}$.
14	SCL	Serial Input Register Clock Pin. Shifts in one bit at a time upon positive clock edges. $V_{SCL} \le (V_{DD} + 0.3$ V). Pull-up resistor is recommended for SCL to ensure minimum power.
15	DGND	Digital Ground. Connect to system analog ground at a single point.
16	AD1	I^2C Device Address 1. AD0 and AD1 allow four AD5253/AD5254 devices to be addressed.
17	A3	A Terminal of RDAC3. $V_{SS} \le V_{A3} \le V_{DD}$.
18	B3	B Terminal of RDAC3. $V_{SS} \le V_{B3} \le V_{DD}$.
19	W3	Wiper Terminal of RDAC3. $V_{SS} \le V_{W3} \le V_{DD}$.
20	V_{DD}	Positive Power Supply Pin. Connect +2.7 V to +5 V for single supply or ±2.7 V for dual supply, where $V_{DD} - V_{SS} \le +5.5$ V. V_{DD} must be able to source 35 mA for 26 ms when storing data to EEMEM.

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TYPICAL PERFORMANCE CHARACTERISTICS

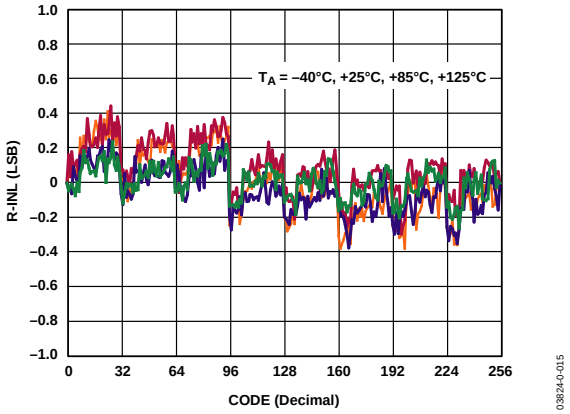

Figure 3. R-INL vs. Code

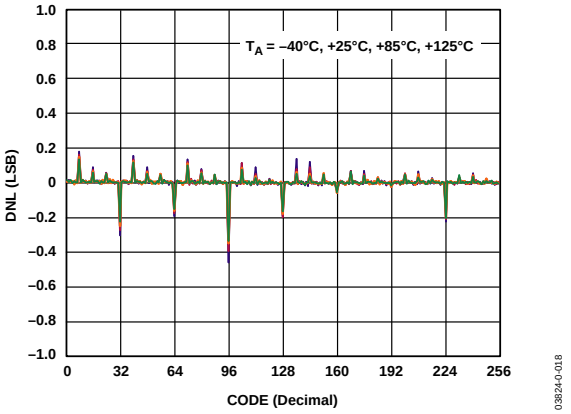

Figure 6. DNL vs. Code

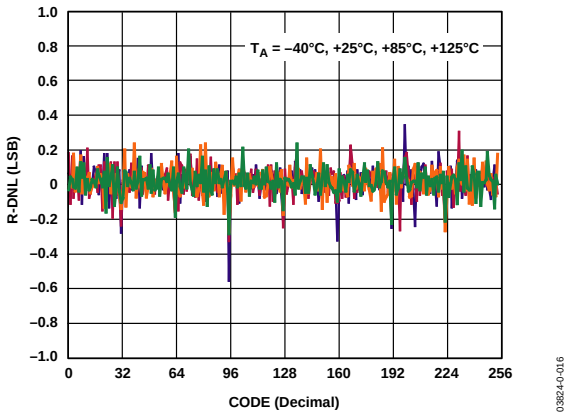

Figure 4. R-DNL vs. Code

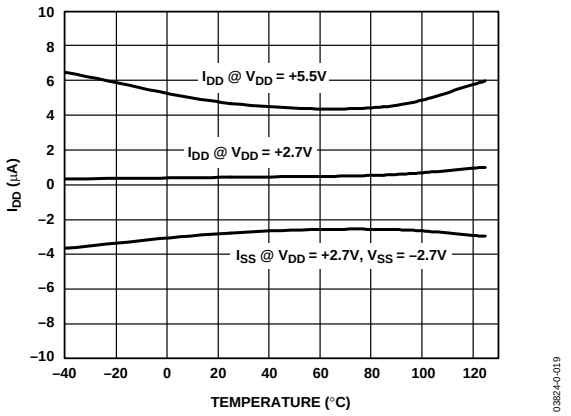

Figure 7. Supply Current vs. Temperature

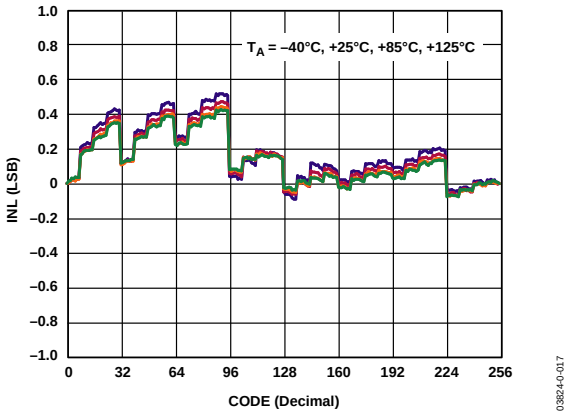

Figure 5. INL vs. Code

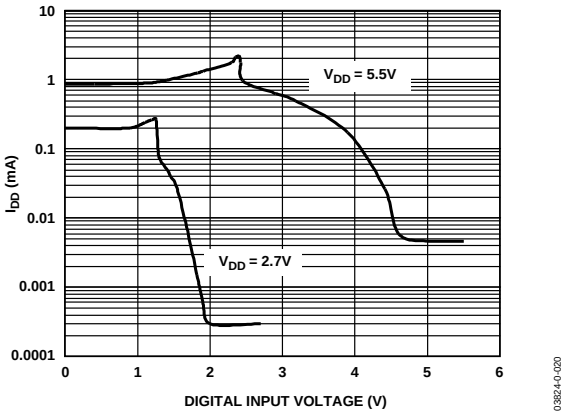

Figure 8. Supply Current vs. Digital Input Voltage, T_A = 25°C

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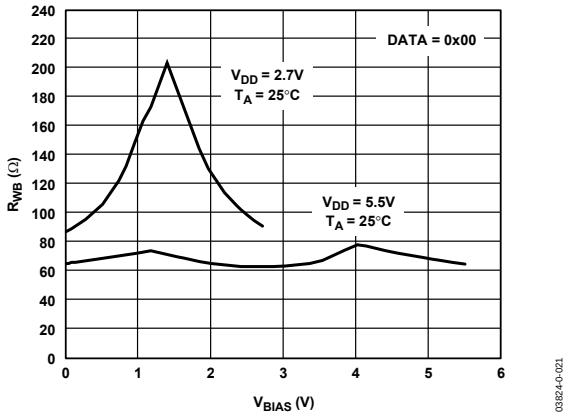

Figure 9. Wiper Resistance vs. V_{BIAS}

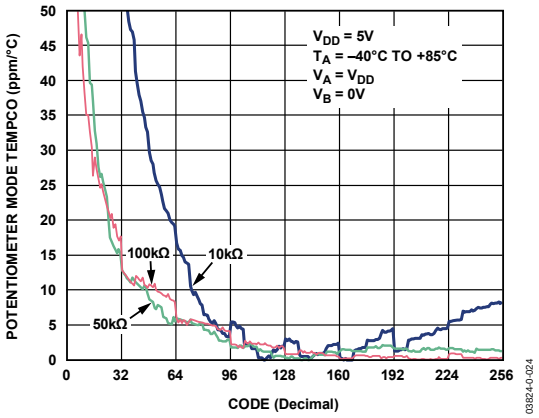

Figure 12. Potentiometer Mode Tempco ($\Delta V_{WB}/V_{WB})/\Delta T \times 10^6$ vs. Code

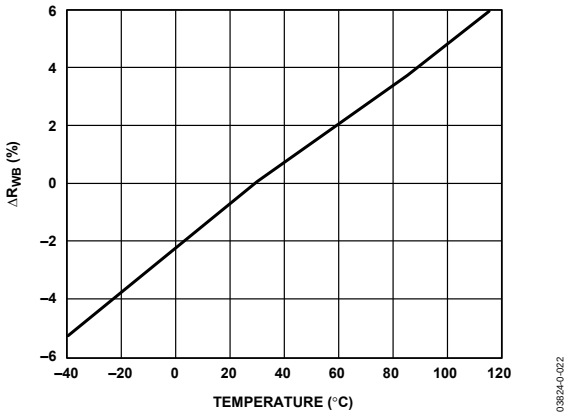

Figure 10. Change of R_{WB} vs. Temperature

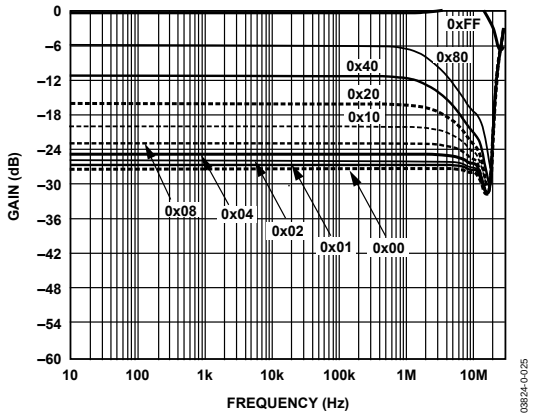

Figure 13. Gain vs. Frequency vs. Code, R_{AB} = 1 kΩ, T_A = 25°C

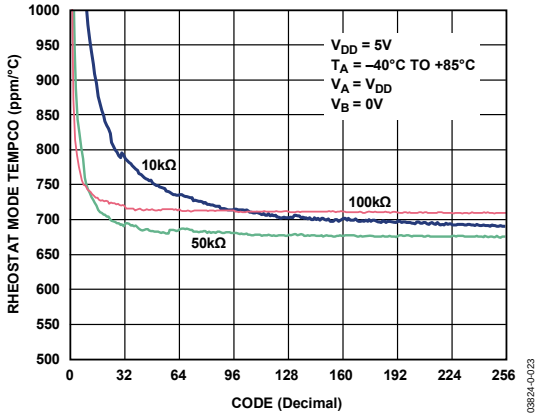

Figure 11. Rheostat Mode Tempco ($\Delta R_{WB}/R_{WB})/\Delta T \times 10^6$ vs. Code

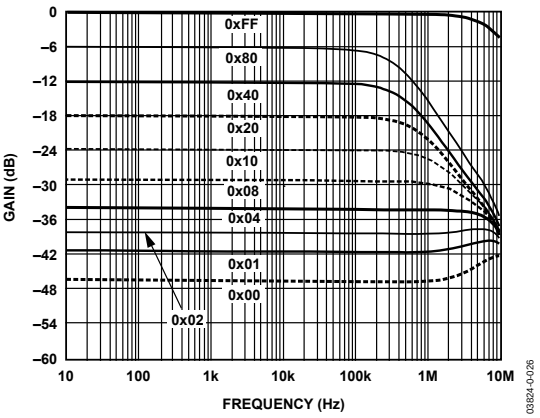

Figure 14. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ, T_A = 25°C

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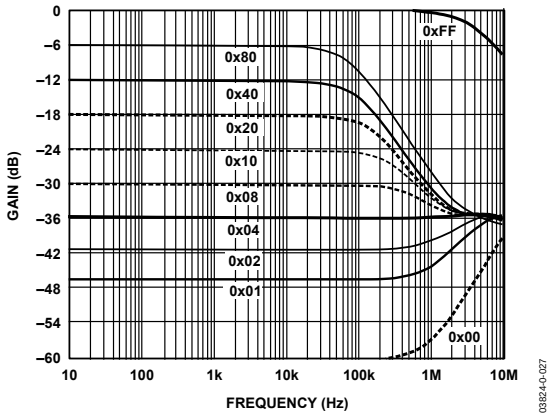

Figure 15. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ, T_A = 25°C

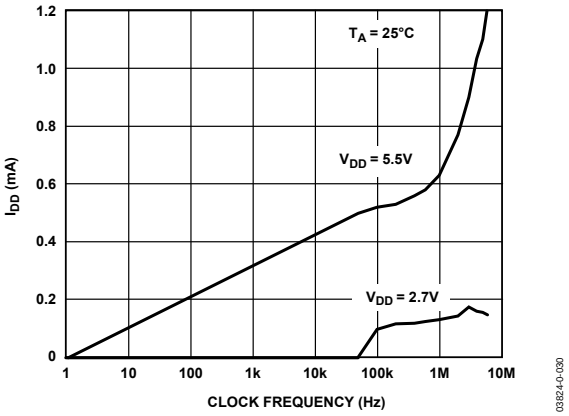

Figure 18. Supply Current vs. Digital Input Clock Frequency

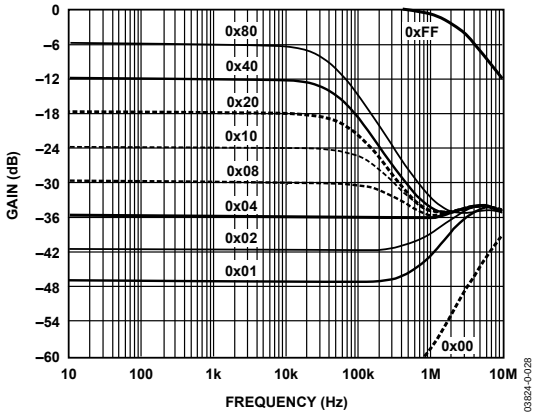

Figure 16. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ, T_A = 25°C

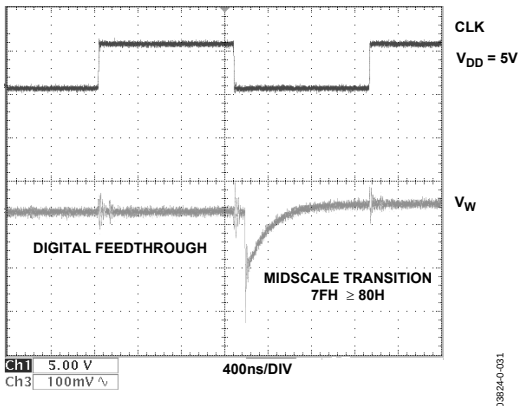

Figure 19. Clock Feedthrough and Midscale Transition Glitch

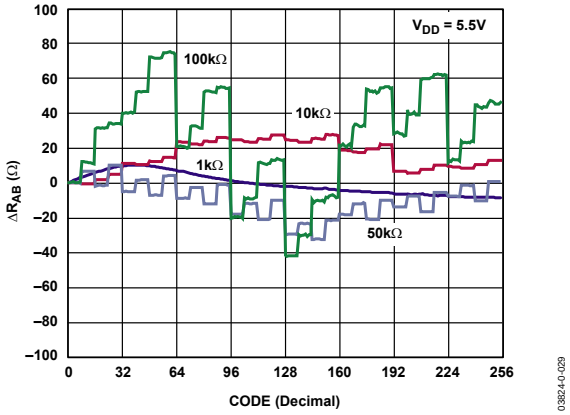

Figure 17. ΔR_{AB} vs. Code, T_A = 25°C

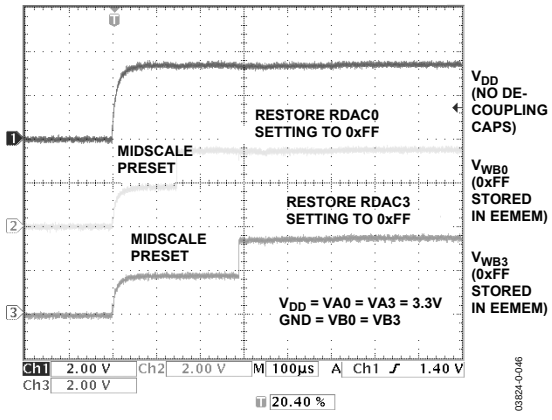

Figure 20. $t_{EEMEM_RESTORE}$ of RDAC0 and RDAC3

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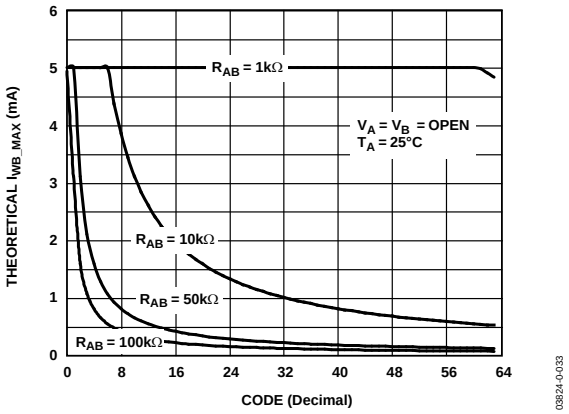

Figure 21. AD5253 I_{WB_MAX} vs. Code

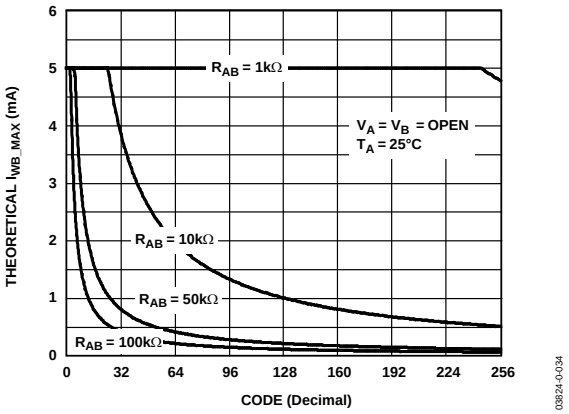

Figure 22. AD5254 I_{WB_MAX} vs. Code

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I²C INTERFACE

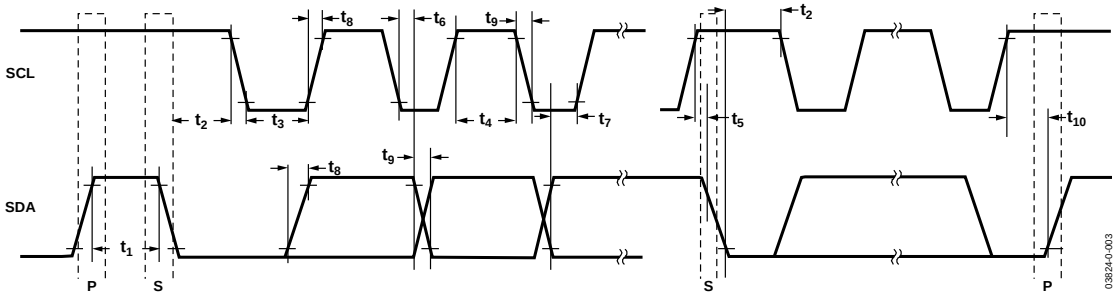

Figure 23. I²C Interface Timing Diagram

I²C INTERFACE GENERAL DESCRIPTION

From Master to Slave

From Slave to Master

S = start condition
P = stop condition
A = acknowledge (SDA low)
$\overline{A}$ = not acknowledge (SDA high)
R/$\overline{W}$ = read enable at high; write enable at low

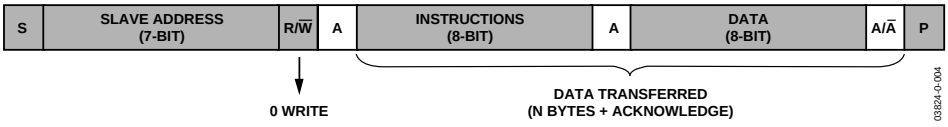

Figure 24. I²C—Master Writing Data to Slave

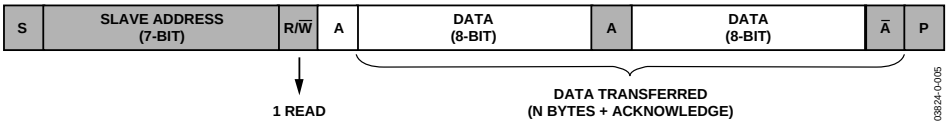

Figure 25. I²C—Master Reading Data from Slave

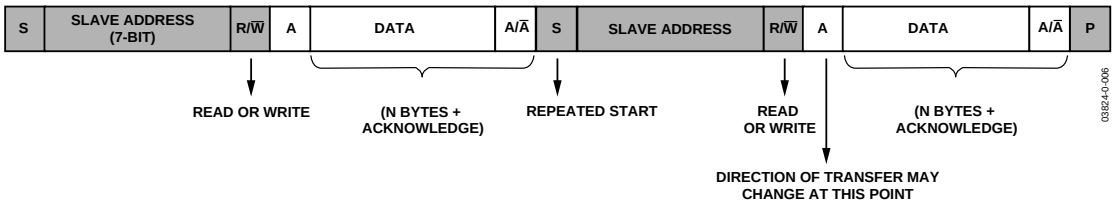

Figure 26. I²C—Combined Write/Read

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I²C INTERFACE DETAIL DESCRIPTION

From Master to Slave

From Slave to Master

S = start condition
P = stop condition
A = acknowledge (SDA low)
$\overline{A}$ = not acknowledge (SDA high)
AD1, AD0 = I²C device address bits, must match with the logic states at Pins AD1, AD0
R/$\overline{W}$= read enable bit at logic high; write enable bit at logic low
CMD/$\overline{REG}$ = command enable bit at logic high; register access bit at logic low
EE/$\overline{RDAC}$ = EEMEM register at logic high; RDAC register at logic low
A4, A3, A2, A1, A0 = RDAC/EEMEM register addresses

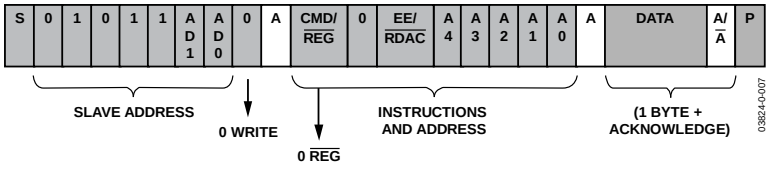

Figure 27. Single Write Mode

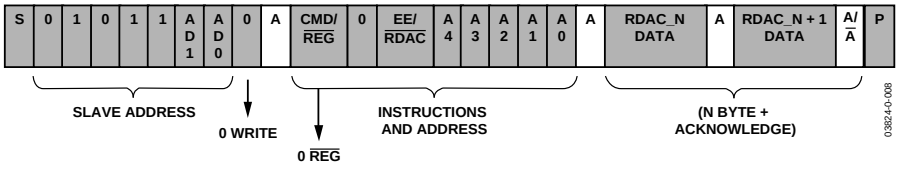

Figure 28. Consecutive Write Mode

Table 6. Addresses for Writing Data Byte Contents to RDAC Registers (R/$\overline{W}$ = 0, CMD/$\overline{REG}$ = 0, EE/$\overline{RDAC}$ = 0)

A4	*A3*	*A2*	*A1*	*A0*	RDAC	Data Byte Description
0	0	0	0	0	RDAC0	6-/8-bit wiper setting (2 MSB of AD5253 are X)
0	0	0	0	1	RDAC1	6-/8-bit wiper setting (2 MSB of AD5253 are X)
0	0	0	1	0	RDAC2	6-/8-bit wiper setting (2 MSB of AD5253 are X)
0	0	0	1	1	RDAC3	6-/8-bit wiper setting (2 MSB of AD5253 are X)
0	0	1	0	0	Reserved	
:	:	:	:	:	:	
:	:	:	:	:	:	
0	1	1	1	1	Reserved	

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RDAC/EEMEM Write

Setting the wiper position requires an RDAC write operation. The single write operation is shown in Figure 27, and the consecutive write operation is shown in Figure 28. In the consecutive write operation, if the $\overline{\text{RDAC}}$ is selected and the address starts at 0, the first data byte goes to RDAC0, the second data byte goes to RDAC1, the third data byte goes to RDAC2, and the fourth data byte goes to RDAC3. This operation can be continued for up to eight addresses with four unused addresses; it then loops back to RDAC0. If the address starts at any of the eight valid addresses, N, the data first goes to RDAC_N, RDAC_N + 1, and so on; it loops back to RDAC0 after the eighth address. The RDAC address is shown in Table 6.

While the RDAC wiper setting is controlled by a specific RDAC register, each RDAC register corresponds to a specific EEMEM location, which provides nonvolatile wiper storage functionality. The addresses are shown in Table 7. The single and consecutive write operations also apply to EEMEM write operations.

There are 12 nonvolatile memory locations: EEMEM4 to EEMEM15. Users can store 12 bytes of information, such as memory data for other components, look-up tables, or system identification information.

In a write operation to the EEMEM registers, the device disables the I^2C interface during the internal write cycle. Acknowledge polling is required to determine the completion of the write cycle. See the EEMEM Write-Acknowledge Polling section.

RDAC/EEMEM Read

The AD5253/AD5254 provide two different RDAC or EEMEM read operations. For example, Figure 29 shows the method of reading the RDAC0 to RDAC3 contents without specifying the address, assuming Address RDAC0 was already selected in the previous operation. If an RDAC_N address other than RDAC0 was previously selected, readback starts with Address N, followed by N + 1, and so on.

Figure 30 illustrates a random RDAC or EEMEM read operation. This operation allows users to specify which RDAC or EEMEM register is read by issuing a dummy write command to change the RDAC address pointer and then proceeding with the RDAC read operation at the new address location.

Table 7. Addresses for Writing (Storing) RDAC Settings and User-Defined Data to EEMEM Registers ($R/\overline{W}$ = 0, CMD/$\overline{REG}$ = 0, EE/$\overline{RDAC}$ = 1)

A4	*A3*	*A2*	*A1*	*A0*	Data Byte Description
0	0	0	0	0	Store RDAC0 setting to EEMEM0[1]
0	0	0	0	1	Store RDAC1 setting to EEMEM1[1]
0	0	0	1	0	Store RDAC2 setting to EEMEM2[1]
0	0	0	1	1	Store RDAC3 setting to EEMEM3[1]
0	0	1	0	0	Store user data to EEMEM4
0	0	1	0	1	Store user data to EEMEM5
0	0	1	1	0	Store user data to EEMEM6
0	0	1	1	1	Store user data to EEMEM7
0	1	0	0	0	Store user data to EEMEM8
0	1	0	0	1	Store user data to EEMEM9
0	1	0	1	0	Store user data to EEMEM10
0	1	0	1	1	Store user data to EEMEM11
0	1	1	0	0	Store user data to EEMEM12
0	1	1	0	1	Store user data to EEMEM13
0	1	1	1	0	Store user data to EEMEM14
0	1	1	1	1	Store user data to EEMEM15

Table 8. Addresses for Reading (Restoring) RDAC Settings and User Data from EEMEM ($R/\overline{W}$ = 1, CMD/$\overline{REG}$ = 0, EE/$\overline{RDAC}$ = 1)

A4	*A3*	*A2*	*A1*	*A0*	Data Byte Description
0	0	0	0	0	Read RDAC0 setting from EEMEM0
0	0	0	0	1	Read RDAC1 setting from EEMEM1
0	0	0	1	0	Read RDAC2 setting from EEMEM2
0	0	0	1	1	Read RDAC3 setting from EEMEM3
0	0	1	0	0	Read User data from EEMEM4
0	0	1	0	1	Read user data from EEMEM5
0	0	1	1	0	Read user data from EEMEM6
0	0	1	1	1	Read user data from EEMEM7
0	1	0	0	0	Read user data from EEMEM8
0	1	0	0	1	Read user data from EEMEM9
0	1	0	1	0	Read user data from EEMEM10
0	1	0	1	1	Read user data from EEMEM11
0	1	1	0	0	Read user data from EEMEM12
0	1	1	0	1	Read user data from EEMEM13
0	1	1	1	0	Read user data from EEMEM14
0	1	1	1	1	Read user data from EEMEM15

[1] Users can store any of the 64 RDAC settings for AD5253 or any of the 256 RDAC settings for the AD5254 directly to the EEMEM. This is not limited to current RDAC wiper setting.

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From Master to Slave

From Slave to Master

S = start condition
P = stop condition
$\underline{A}$ = acknowledge (SDA low)
$\overline{A}$ = not acknowledge (SDA high)
AD1, AD0 = I^2C device address bits, must match with the logic states at Pins AD1, AD0
R/$\overline{W}$ = read enable bit at logic high; write enable bit at logic low
CMD/$\overline{REG}$ = command enable bit at logic high; register access bit at logic low
C3, C2, C1, C0 = command bits
A2, A1, A0 = RDAC/EEMEM register addresses

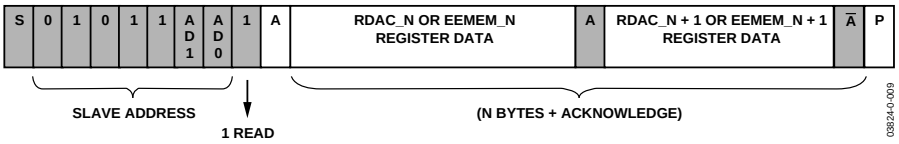

Figure 29. RDAC Current Read (Restricted to Previously Selected Address Stored in the Register)

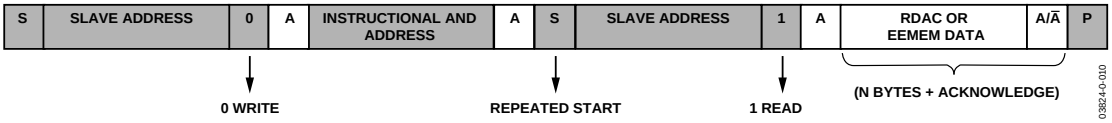

Figure 30. RDAC or EEMEM Random Read

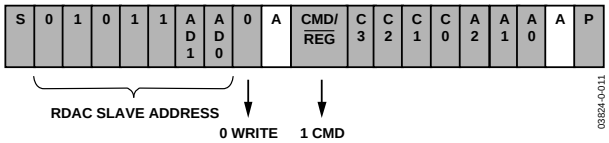

Figure 31. RDAC Quick Command Write (Dummy Write)

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RDAC/EEMEM Quick Commands

The AD5253/AD5254 feature 12 quick commands that facilitate easy manipulation of RDAC wiper settings and provide RDAC-to-EEMEM storing and restoring functions. The command format is shown in Figure 31, and the command descriptions are shown in Table 9.

When using a quick command, issuing a third byte is not needed, but is allowed. The quick commands reset and store RDAC to EEMEM require acknowledge polling to determine whether the command has finished executing.

R_{AB} Tolerance Stored in Read-Only Memory

The AD5253/AD5254 feature patented R_{AB} tolerances storage in the nonvolatile memory. The tolerance of each channel is stored in the memory during the factory production and can be read by users at any time. The knowledge of the stored tolerance, which is the average of R_{AB} over all codes (see Figure 16), allows users to predict R_{AB} accurately. This feature is valuable for precision, rheostat mode, and open-loop applications, in which knowledge of absolute resistance is critical.

The stored tolerances reside in the read-only memory and are expressed as percentages. Each tolerance is 16 bits long and is stored in two memory locations (see Table 10). The tolerance data is expressed in sign magnitude binary format stored in two bytes; an example is shown in Figure 32 . For the first byte in Register N, the MSB is designated for the sign (0 = + and 1 = –) and the 7 LSB is designated for the integer portion of the tolerance. For the second byte in Register N + 1, all eight data bits are designated for the decimal portion of tolerance. As shown in Table 10 and Figure 32, for example, if the rated R_{AB} is 10 kΩ and the data readback from Address 11000 shows 0001 1100 and Address 11001 shows 0000 1111, then RDAC0 tolerance can be calculated as

MSB: 0 = +
Next 7 MSB: 001 1100 = 28
8 LSB: 0000 1111 = 15×2^{-8} = 0.06
Tolerance = 28.06% and, therefore,
R_{AB_ACTUAL} = 12.806 kΩ

EEMEM Write-Acknowledge Polling

After each write operation to the EEMEM registers, an internal write cycle begins. The I^2C interface of the device is disabled. To determine if the internal write cycle is complete and the I^2C interface is enabled, interface polling can be executed. I^2C interface polling can be conducted by sending a start condition followed by the slave address and the write bit. If the I^2C interface responds with an ACK, the write cycle is complete and the interface is ready to proceed with further operations. Otherwise, I^2C interface polling can be repeated until it succeeds. Command 2 and Command 7 also require acknowledge polling.

EEMEM Write Protection

Setting the $\overline{WP}$ pin to logic low after EEMEM programming protects the memory and RDAC registers from future write operations. In this mode, the EEMEM and RDAC read operations function as normal.

Table 9. RDAC-to-EEMEM Interface and RDAC Operation Quick Command Bits (CMD/$\overline{REG}$ = 1, A2 = 0)

C3	C2	C1	C0	Command Description
0	0	0	0	NOP
0	0	0	1	Restore EEMEM (A1, A0) to RDAC (A1, A0)[1]
0	0	1	0	Store RDAC (A1, A0) to EEMEM (A1, A0)
0	0	1	1	Decrement RDAC (A1, A0) 6 dB
0	1	0	0	Decrement all RDACs 6 dB
0	1	0	1	Decrement RDAC (A1, A0) one step
0	1	1	0	Decrement all RDACs one step
0	1	1	1	Reset: restore EEMEMs to all RDACs
1	0	0	0	Increment RDACs (A1, A0) 6 dB
1	0	0	1	Increment all RDACs 6 dB
1	0	1	0	Increment RDACs (A1, A0) one step
1	0	1	1	Increment all RDACs one step
1	1	0	0	Reserved
:	:	:	:	:
:	:	:	:	:
1	1	1	1	Reserved

[1] This command leaves the device in the EEMEM read power state, which consumes power. Issue the NOP command to return the device to its idle state.

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Table 10. Address Table for Reading Tolerance (CMD/$\overline{\text{REG}}$ = 0, EE/$\overline{\text{RDAC}}$ = 1, A4 = 1)

A4	A3	A2	A1	A0	Data Byte Description
1	1	0	0	0	Sign and 7-bit integer values of RDAC0 tolerance (read only)
1	1	0	0	1	8-bit decimal value of RDAC0 tolerance (read only)
1	1	0	1	0	Sign and 7-bit integer values of RDAC1 tolerance (read only)
1	1	0	1	1	8-bit decimal value of RDAC1 tolerance (read only)
1	1	1	0	0	Sign and 7-bit integer values of RDAC2 tolerance (read only)
1	1	1	0	1	8-bit decimal value of RDAC2 tolerance (read only)
1	1	1	1	0	Sign and 7-bit integer values of RDAC3 tolerance (read only)
1	1	1	1	1	8-bit decimal value of RDAC3 tolerance (read only)

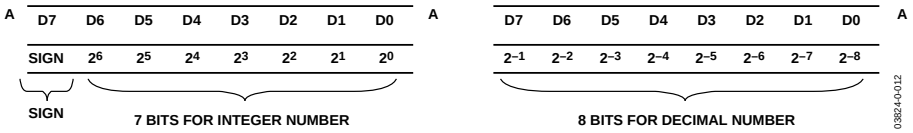

Figure 32. Format of Stored Tolerance in Sign Magnitude Format with Bit Position Descriptions (Unit is Percent, Only Data Bytes Are Shown)

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I²C-COMPATIBLE 2-WIRE SERIAL BUS

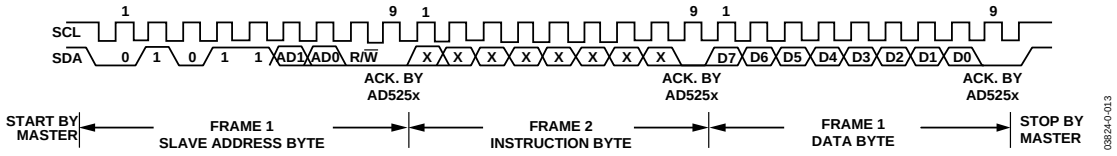

Figure 33. General I²C Write Pattern

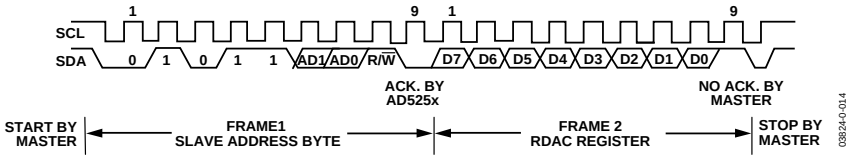

Figure 34. General I²C Read Pattern

The first byte of the AD5253/AD5254 is a slave address byte (see Figure 33 and Figure 34). It has a 7-bit slave address and an R/$\overline{W}$ bit. The 5 MSB of the slave address is 01011, and the next 2 LSB is determined by the states of the AD1 and AD0 pins. AD1 and AD0 allow the user to place up to four AD5253/AD5254 devices on one bus.

AD5253/AD5254 can be controlled via an I²C-compatible serial bus and are connected to this bus as slave devices. The 2-wire I²C serial bus protocol (see Figure 33 and Figure 34) follows:

1. The master initiates a data transfer by establishing a start condition, such that SDA goes from high to low while SCL is high (see Figure 33). The following byte is the slave address byte, which consists of the 5 MSB of a slave address defined as 01011. The next two bits are AD1 and AD0, I²C device address bits. Depending on the states of their AD1 and AD0 bits, four AD5253/AD5254 devices can be addressed on the same bus. The last LSB, the R/$\overline{W}$ bit, determines whether data is read from or written to the slave device.

   The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is called an acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register.

2. In the write mode (except when restoring EEMEM to the RDAC register), there is an instruction byte that follows the slave address byte. The MSB of the instruction byte is labeled CMD/$\overline{REG}$. MSB = 1 enables CMD, the command instruction byte; MSB = 0 enables general register writing. The third MSB in the instruction byte, labeled EE/$\overline{RDAC}$, is true when MSB = 0 or when the device is in general writing mode. EE enables the EEMEM register, and REG enables the RDAC register. The 5 LSB, A4 to A0, designates the addresses of the EEMEM and RDAC registers (see Figure 27 and Figure 28). When MSB = 1 or when the device is in CMD mode, the four bits following the MSB are C3 to C1, which correspond to 12 predefined EEMEM controls and quick commands; there are also four factory-reserved commands. The 3 LSB—A2, A1, and A0—are 4-channel RDAC addresses (see Figure 31). After acknowledging the instruction byte, the last byte in the write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 33).

3. In current read mode, the RDAC0 data byte immediately follows the acknowledgment of the slave address byte. After an acknowledgement, RDAC1 follows, then RDAC2, and so on. (There is a slight difference in write mode, where the last eight data bits representing RDAC3 data are followed by a no acknowledge bit.) Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 34). Another reading method, random read method, is shown in Figure 30.

4. When all data bits have been read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line that occurs while SCL is high. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition (see Figure 33). In read mode, the master issues a no acknowledge for the ninth clock pulse, that is, the SDA line remains high. The master brings the SDA line low before the 10th clock pulse and then brings the SDA line high to establish a stop condition (see Figure 34).

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THEORY OF OPERATION

The AD5253/AD5254 are quad-channel digital potentiometers in 1 kΩ, 10 kΩ, 50 kΩ, or 100 kΩ that allow 64/256 linear resistance step adjustments. The AD5253/AD5254 employ double-gate CMOS EEPROM technology, which allows resistance settings and user-defined data to be stored in the EEMEM registers. The EEMEM is nonvolatile, such that settings remain when power is removed. The RDAC wiper settings are restored from the nonvolatile memory settings during device power-up and can also be restored at any time during operation.

The AD5253/AD5254 resistor wiper positions are determined by the RDAC register contents. The RDAC register acts like a scratch-pad register, allowing unlimited changes of resistance settings. RDAC register contents can be changed using the device's serial I^2C interface. The format of the data-words and the commands to program the RDAC registers are discussed in the I^2C Interface section.

The four RDAC registers have corresponding EEMEM memory locations that provide nonvolatile storage of resistor wiper position settings. The AD5253/AD5254 provide commands to store the RDAC register contents to their respective EEMEM memory locations. During subsequent power-on sequences, the RDAC registers are automatically loaded with the stored value.

Whenever the EEMEM write operation is enabled, the device activates the internal charge pump and raises the EEMEM cell gate bias voltage to a high level; this essentially erases the current content in the EEMEM register and allows subsequent storage of the new content. Saving data to an EEMEM register consumes about 35 mA of current and lasts approximately 26 ms. Because of charge-pump operation, all RDAC channels may experience noise coupling during the EEMEM writing operation.

The EEMEM restore time in power-up or during operation is about 300 µs. Note that the power-up EEMEM refresh time depends on how fast V_{DD} reaches its final value. As a result, any supply voltage decoupling capacitors limit the EEMEM restore time during power-up. For example, Figure 20 shows the power-up profile of the V_{DD} where there is no decoupling capacitors and the applied power is a digital signal. The device initially resets the RDACs to midscale before restoring the EEMEM contents. The omission of the decoupling capacitors should only be considered when the fast restoring time is absolutely needed in the application. In addition, users should issue a NOP Command 0 immediately after using Command 1 to restore the EEMEM setting to RDAC, thereby minimizing supply current dissipation. Reading user data directly from EEMEM does not require a similar NOP command execution.

In addition to the movement of data between RDAC and EEMEM registers, the AD5253/AD5254 provide other shortcut commands that facilitate programming, as shown in Table 11.

Table 11. Quick Commands

Command	Description
0	NOP.
1	Restore EEMEM content to RDAC. User should issue NOP immediately after this command to conserve power.
2	Store RDAC register setting to EEMEM.
3	Decrement RDAC 6 dB (shift data bits right).
4	Decrement all RDACs 6 dB (shift all data bits right).
5	Decrement RDAC one step.
6	Decrement all RDACs one step.
7	Reset EEMEM contents to all RDACs.
8	Increment RDAC 6 dB (shift data bits left).
9	Increment all RDACs 6 dB (shift all data bits left).
10	Increment RDAC one step.
11	Increment all RDACs one step.
12 to 15	Reserved.

LINEAR INCREMENT/DECREMENT COMMANDS

The increment and decrement commands (10, 11, 5, and 6) are useful for linear step-adjustment applications. These commands simplify microcontroller software coding by allowing the controller to send just an increment or decrement command to the AD5253/AD5254. The adjustments can be directed to a single RDAC or to all four RDACs.

±6 dB ADJUSTMENTS (DOUBLING/HALVING WIPER SETTING)

The AD5253/AD5254 accommodate ±6 dB adjustments of the RDAC wiper positions by shifting the register contents to left/right for increment/decrement operations, respectively. Command 3, Command 4, Command 8, and Command 9 can be used to increment or decrement the wiper positions in 6 dB steps synchronously or asynchronously.

Incrementing the wiper position by +6 dB essentially doubles the RDAC register value, whereas decrementing the wiper position by –6 dB halves the register content. Internally, the AD5253/AD5254 use shift registers to shift the bits left and right to achieve a ±6 dB increment or decrement. The maximum number of adjustments is nine and eight steps for incrementing from zero scale and decrementing from full scale, respectively. These functions are useful for various audio/video level adjustments, especially for white LED brightness settings in which human visual responses are more sensitive to large adjustments than to small adjustments.

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AD5253/AD5254 Data Sheet

DIGITAL INPUT/OUTPUT CONFIGURATION

SDA is a digital input/output with an open-drain MOSFET that requires a pull-up resistor for proper communication. On the other hand, SCL and $\overline{WP}$ are digital inputs for which pull-up resistors are recommended to minimize the MOSFET cross-conduction current when the driving signals are lower than V_{DD}. SCL and $\overline{WP}$ have ESD protection diodes, as shown in Figure 35 and Figure 36.

$\overline{WP}$ can be permanently tied to V_{DD} without a pull-up resistor if the write-protect feature is not used. If $\overline{WP}$ is left floating, an internal current source pulls it low to enable write protection. In applications in which the device is programmed infrequently, this allows the part to default to write-protection mode after any one-time factory programming or field calibration without using an on-board pull-down resistor. Because there are protection diodes on all inputs, the signal levels must not be greater than V_{DD} to prevent forward biasing of the diodes.

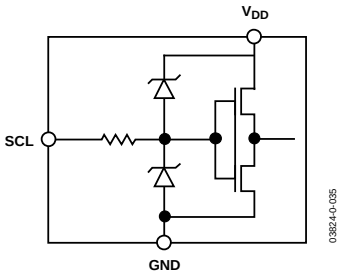

Figure 35. SCL Digital Input

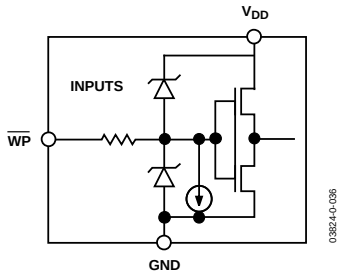

Figure 36. Equivalent $\overline{WP}$ Digital Input

MULTIPLE DEVICES ON ONE BUS

The AD5253/AD5254 are equipped with two addressing pins, AD1 and AD0, that allow up to four AD5253/AD5254 devices to be operated on one I^2C bus. To achieve this result, the states of AD1 and AD0 on each device must first be defined. An example is shown in Table 12 and Figure 37. In I^2C programming, each device is issued a different slave address—01011(AD1)(AD0)—to complete the addressing.

Table 12. Multiple Devices Addressing

AD1	AD0	Device Addressed
0	0	U1
0	1	U2
1	0	U3
1	1	U4

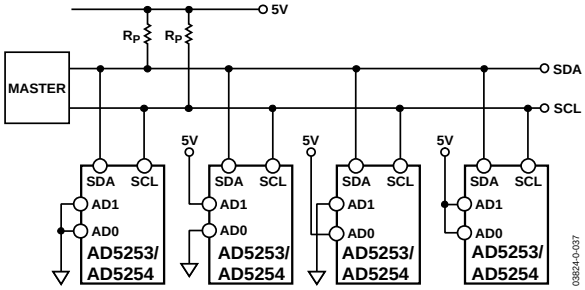

Figure 37. Multiple AD5253/AD5254 Devices on a Single Bus

In wireless base station smart-antenna systems that require arrays of digital potentiometers to bias the power amplifiers, large numbers of AD5253/AD5254 devices can be addressed by using extra decoders, switches, and I/O buses, as shown in Figure 38. For example, to communicate to a total of 16 devices, four decoders and 16 sets of combinational switches (four sets shown in Figure 38) are needed. Two I/O buses serve as the common inputs of the four 2 × 4 decoders and select four sets of outputs at each combination. Because the four sets of combination switch outputs are unique, as shown in Figure 38, a specific device is addressed by properly programming the I^2C with the slave address defined as 01011(AD1)(AD0). This operation allows one of 16 devices to be addressed, provided that the inputs of the two decoders do not change states. The inputs of the decoders are allowed to change once the operation of the specified device is completed.

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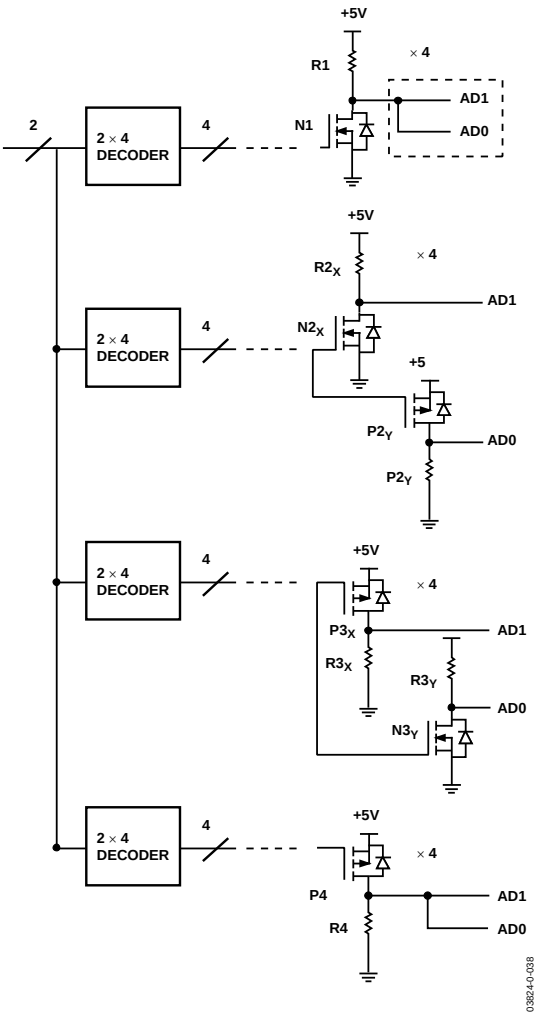

Figure 38. Four Devices with AD1 and AD0 of 00

TERMINAL VOLTAGE OPERATION RANGE

The AD5253/AD5254 are designed with internal ESD diodes for protection; these diodes also set the boundaries for the terminal operating voltages. Positive signals present on Terminal A, Terminal B, or Terminal W that exceed V_{DD} are clamped by the forward-biased diode. Similarly, negative signals on Terminal A, Terminal B, or Terminal W that are more negative than V_{SS} are also clamped (see Figure 39). In practice, users should not operate V_{AB}, V_{WA}, and V_{WB} to be higher than the voltage across V_{DD} to V_{SS}, but V_{AB}, V_{WA}, and V_{WB} have no polarity constraint.

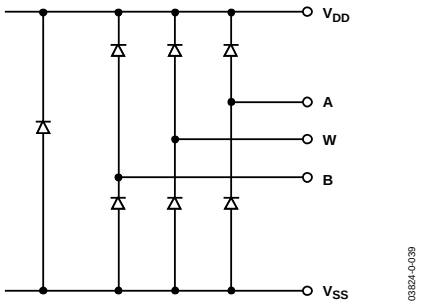

Figure 39. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

POWER-UP AND POWER-DOWN SEQUENCES

Because the ESD protection diodes limit the voltage compliance at Terminal A, Terminal B, and Terminal W (Figure 39), it is important to power V_{DD}/V_{SS} before applying any voltage to these terminals. Otherwise, the diodes are forward biased such that V_{DD}/V_{SS} are powered unintentionally and may affect the user's circuit. Similarly, V_{DD}/V_{SS} should be powered down last. The ideal power-up sequence is in the following order: GND, V_{DD}, V_{SS}, digital inputs, and $V_A/V_B/V_W$. The order of powering V_A, V_B, V_W, and the digital inputs is not important, as long as they are powered after V_{DD}/V_{SS}.

LAYOUT AND POWER SUPPLY BIASING

It is always a good practice to employ a compact, minimum lead-length layout design. The leads to the input should be as direct as possible, with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also good practice to bypass the power supplies with quality capacitors. Low equivalent series resistance (ESR) 1 µF to 10 µF tantalum or electrolytic capacitors should be applied at the supplies to minimize any transient disturbance and filter low frequency ripple. Figure 40 illustrates the basic supply-bypassing configuration for the AD5253/AD5254.

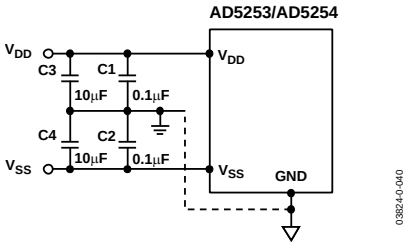

Figure 40. Power Supply-Bypassing Configuration

The ground pin of the AD5253/AD5254 is used primarily as a digital ground reference. To minimize the digital ground bounce, the AD5253/AD5254 ground terminal should be joined remotely to the common ground (see Figure 40).

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DIGITAL POTENTIOMETER OPERATION

The structure of the RDAC is designed to emulate the performance of a mechanical potentiometer. The RDAC contains a string of resistor segments with an array of analog switches that act as the wiper connection to the resistor array. The number of points is the resolution of the device. For example, the AD5253/AD5254 emulate 64/256 connection points with 64/256 equal resistance, R_S, allowing them to provide better than 1.5%/0.4% resolution.

Figure 41 provides an equivalent diagram of the connections between the three terminals that make up one channel of the RDAC. Switches SW_A and SW_B are always on, but only one of switches SW(0) to SW(2^{N-1}) can be on at a time (determined by the setting decoded from the data bit). Because the switches are nonideal, there is a 75 Ω wiper resistance, R_W. Wiper resistance is a function of supply voltage and temperature: Lower supply voltages and higher temperatures result in higher wiper resistances. Consideration of wiper resistance dynamics is important in applications in which accurate prediction of output resistance is required.

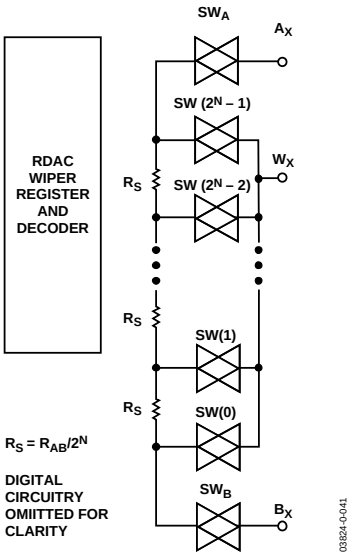

Figure 41. Equivalent RDAC Structure

PROGRAMMABLE RHEOSTAT OPERATION

If either the W-to-B or W-to-A terminal is used as a variable resistor, the unused terminal can be opened or shorted with W; such operation is called rheostat mode (see Figure 42). The resistance tolerance can range ±20%.

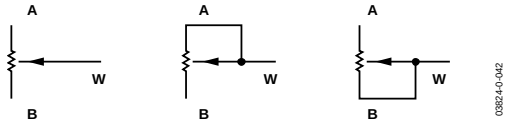

Figure 42. Rheostat Mode Configuration

The nominal resistance of the AD5253/AD5254 has 64/256 contact points accessed by the wiper terminal, plus the B terminal contact. The 6-/8-bit data-word in the RDAC register is decoded to select one of the 64/256 settings. The wiper's first connection starts at the B terminal for Data 0x00. This B terminal connection has a wiper contact resistance, R_W, of 75 Ω, regardless of the nominal resistance. The second connection (the AD5253 10 kΩ part) is the first tap point where R_{WB} = 231 Ω ($R_{WB} = R_{AB}/64 + R_W$ = 156 Ω + 75 Ω) for Data 0x01, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at R_{WB} = 9893 Ω. See Figure 41 for a simplified diagram of the equivalent RDAC circuit.

The general equation that determines the digitally programmed output resistance between W and B is

$$\text{AD5253: RWB(D)} = (D/64) \times \text{RAB} + 75\ \Omega \quad (1)$$

$$\text{AD5254: RWB(D)} = (D/256) \times \text{RAB} + 75\ \Omega \quad (2)$$

where:
D is the decimal equivalent of the data contained in the RDAC latch.
R_{AB} is the nominal end-to-end resistance.

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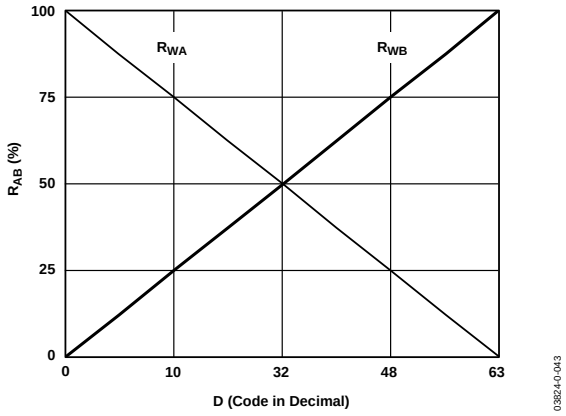

Figure 43. AD5253 $R_{WA}(D)$ and $R_{WB}(D)$ vs. Decimal Code

Since the digital potentiometer is not ideal, a 75 Ω finite wiper resistance is present that can easily be seen when the device is programmed at zero scale. Because of the fine geometric and interconnects employed by the device, care should be taken to limit the current conduction between W and B to no more than ±5 mA continuous for a total resistance of 1 kΩ or a pulse of ±20 mA to avoid degradation or possible destruction of the device. The maximum dc current for AD5253 and AD5254 are shown in Figure 21 and Figure 22, respectively.

Similar to the mechanical potentiometer, the resistance of the RDAC between Wiper W and Terminal A also produces a digitally controlled complementary resistance, R_{WA}. When these terminals are used, the B terminal can be opened. The R_{WA} starts at a maximum value and decreases as the data loaded into the latch increases in value (see Figure 43. The general equation for this operation is

AD5253: RWA(D) = [(64 – D)/64] × RAB + 75 Ω (3)

AD5254: RWA(D) = [(256 – D)/256] × RAB + 75 Ω (4)

The typical distribution of R_{AB} from channel-to-channel matches is about ±0.15% within a given device. On the other hand, device-to-device matching is process-lot dependent with a ±20% tolerance.

PROGRAMMABLE POTENTIOMETER OPERATION

If all three terminals are used, the operation is called potentiometer mode (see Figure 44); the most common configuration is the voltage divider operation.

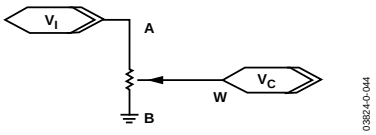

Figure 44. Potentiometer Mode Configuration

If the wiper resistance is ignored, the transfer function is simply

$$\text{AD5253: } V_W = \frac{D}{64} \times V_{AB} + V_B \quad (5)$$

$$\text{AD5254: } V_W = \frac{D}{256} \times V_{AB} + V_B \quad (6)$$

A more accurate calculation that includes the wiper resistance effect is

$$V_W(D) = \frac{\frac{D}{2^N} R_{AB} + R_W}{R_{AB} + 2R_W} V_A \quad (7)$$

where 2^N is the number of steps.

Unlike in rheostat mode operation, where the tolerance is high, potentiometer mode operation yields an almost ratiometric function of $D/2^N$ with a relatively small error contributed by the R_W terms. Therefore, the tolerance effect is almost cancelled. Similarly, the ratiometric adjustment also reduces the temperature coefficient effect to 50 ppm/°C, except at low value codes where R_W dominates.

Potentiometer mode operations include other applications such as op amp input, feedback-resistor networks, and other voltage-scaling applications. The A, W, and B terminals can, in fact, be input or output terminals, provided that $|V_A|$, $|V_W|$, and $|V_B|$ do not exceed V_{DD} to V_{SS}.

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APPLICATIONS INFORMATION

RGB LED BACKLIGHT CONTROLLER FOR LCD PANELS

Because high power (>1 W) RGB LEDs offer superior color quality compared with cold cathode florescent lamps (CCFLs) as backlighting sources, it is likely that high-end LCD panels will employ RGB LEDs as backlight in the near future. Unlike conventional LEDs, high power LEDs have a forward voltage of 2 V to 4 V and consume more than 350 mA at maximum brightness. The LED brightness is a linear function of the conduction current, but not of the forward voltage. To increase the brightness of a given color, multiple LEDs can be connected in series, rather than in parallel, to achieve uniform brightness. For example, three red LEDs configured in series require an average of 6 V to 12 V headroom, but the circuit operation requires current control. As a result, Figure 45 shows the implementation of one high power RGB LED controller using a AD5254, a boost regulator, an op amp, and power MOSFETs.

The ADP1610 (U2 in Figure 45) is an adjustable boost regulator with its output adjusted by the AD5254's RDAC3. Such an output should be set high enough for proper operation but low enough to conserve power. The ADP1610's 1.2 V band gap reference is buffered to provide the reference level for the voltage dividers set by the AD5254's RDAC0 to RDAC2 and Resistor R2 to Resistor R4. For example, by adjusting the AD5254's RDAC0, the desirable voltage appears across the sense resistors, R_R. If U2's output is set properly, op amp U3A and power MOSFET N1 do whatever is necessary to regulate the current of the loop. As a result, the current through the sense resistor and the red LEDs is

$$I_R = \frac{V_{RR}}{R_R} \quad (8)$$

R8 is needed to prevent oscillation.

In addition to the 256 levels of adjustable current/brightness, users can also apply a PWM signal at U3's $\overline{SD}$ pin to achieve finer brightness resolution or better power efficiency.

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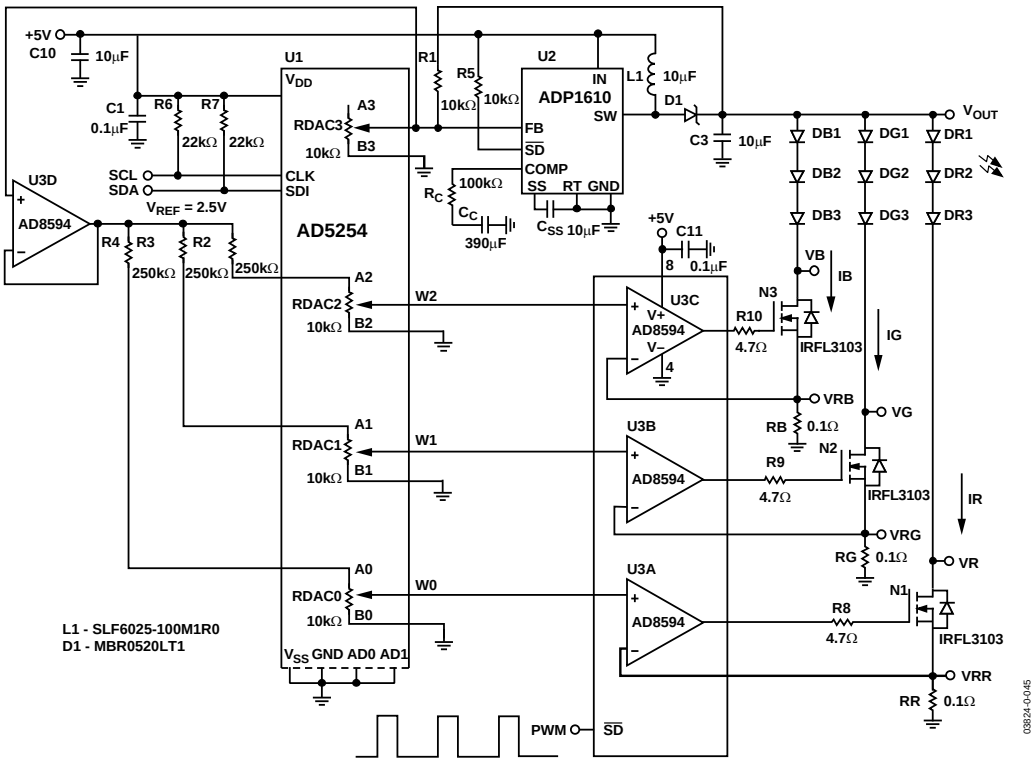

Figure 45. Digital Potentiometer-Based RGB LED Controller

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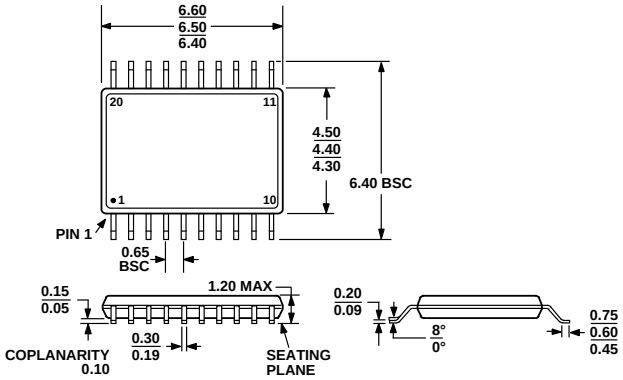
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 46. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters

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ORDERING GUIDE

Model[1, 2, 3]	Step	R_{AB} (kΩ)	Temperature Range	Package Description	Package Option	Ordering Quantity
AD5253BRU1	64	1	−40°C to +105°C	20-Lead TSSOP	RU-20	75
AD5253BRU1-RL7	64	1	−40°C to +105°C	20-Lead TSSOP	RU-20	1,000
AD5253BRUZ1	64	1	−40°C to +105°C	20-Lead TSSOP	RU-20	75
AD5253BRUZ1-RL7	64	1	−40°C to +105°C	20-Lead TSSOP	RU-20	1,000
AD5253BRU10	64	10	−40°C to +105°C	20-Lead TSSOP	RU-20	75
AD5253BRU10-RL7	64	10	−40°C to +105°C	20-Lead TSSOP	RU-20	1,000
AD5253BRUZ10	64	10	−40°C to +105°C	20-Lead TSSOP	RU-20	75
AD5253BRUZ10-RL7	64	10	−40°C to +105°C	20-Lead TSSOP	RU-20	1,000
AD5253BRU50	64	50	−40°C to +105°C	20-Lead TSSOP	RU-20	75
AD5253BRU50-RL7	64	50	−40°C to +105°C	20-Lead TSSOP	RU-20	1,000
AD5253BRUZ50	64	50	−40°C to +105°C	20-Lead TSSOP	RU-20	75
AD5253BRUZ50-RL7	64	50	−40°C to +105°C	20-Lead TSSOP	RU-20	1,000
AD5253BRU100	64	100	−40°C to +105°C	20-Lead TSSOP	RU-20	75
AD5253BRU100-RL7	64	100	−40°C to +105°C	20-Lead TSSOP	RU-20	1,000
AD5253BRUZ100	64	100	−40°C to +105°C	20-Lead TSSOP	RU-20	75
AD5253BRUZ100-RL7	64	100	−40°C to +105°C	20-Lead TSSOP	RU-20	1,000
AD5254BRU1	256	1	−40°C to +105°C	20-Lead TSSOP	RU-20	75
AD5254BRU1-RL7	256	1	−40°C to +105°C	20-Lead TSSOP	RU-20	1,000
AD5254BRUZ1	256	1	−40°C to +105°C	20-Lead TSSOP	RU-20	75
AD5254BRUZ1-RL7	256	1	−40°C to +105°C	20-Lead TSSOP	RU-20	1,000
AD5254BRU10	256	10	−40°C to +105°C	20-Lead TSSOP	RU-20	75
AD5254BRU10-RL7	256	10	−40°C to +105°C	20-Lead TSSOP	RU-20	1,000
AD5254BRUZ10	256	10	−40°C to +105°C	20-Lead TSSOP	RU-20	75
AD5254BRUZ10-RL7	256	10	−40°C to +105°C	20-Lead TSSOP	RU-20	1,000
AD5254BRU50	256	50	−40°C to +105°C	20-Lead TSSOP	RU-20	75
AD5254BRU50-RL7	256	50	−40°C to +105°C	20-Lead TSSOP	RU-20	1,000
AD5254BRUZ50	256	50	−40°C to +105°C	20-Lead TSSOP	RU-20	75
AD5254BRUZ50-RL7	256	50	−40°C to +105°C	20-Lead TSSOP	RU-20	1,000
AD5254BRU100	256	100	−40°C to +105°C	20-Lead TSSOP	RU-20	75
AD5254BRU100-RL7	256	100	−40°C to +105°C	20-Lead TSSOP	RU-20	1,000
AD5254BRUZ100	256	100	−40°C to +105°C	20-Lead TSSOP	RU-20	75
AD5254BRUZ100-RL7	256	100	−40°C to +105°C	20-Lead TSSOP	RU-20	1,000
EVAL-AD5254SDZ	256			Evaluation Board		1

[1] In the package marking, Line 1 shows the part number. Line 2 shows the branding information, such that B1 = 1 kΩ, B10 = 10 kΩ, and so on. There is also a "#" marking for the Pb-free part. Line 3 shows the date code in YYWW.
[2] Z = RoHS Compliant Part.
[3] The evaluation board is shipped with the 10 kΩ R_{AB} resistor option; however, the board is compatible with all available resistor value options.

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